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T184

Case Number: T 88 / 82

DECISION

of the Technical Board of Appeal 3.5.1

of 28 August 1984

Appellant: International Business Machines Corporation
Armonk, N.Y. 10504
USA

Representative: Ahlman, Bertel
IBM Svenska AB Box 962
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Decision under appeal: Decision of Examining Division 067 of the European Patent Office dated 01.03.82 refusing European patent application No 79101908.6 pursuant to Article 97(1) EPC

Composition of the Board:

Chairman: G. Korsakoff

Member: J. van Voorthuizen

Member: P. Ford

Summary of facts and submissions

I. European Patent application 79 101 908.6 filed on 12.06.79 (Publication No. 0 006 531) claiming a priority of 30.06.78 (US) was refused by a decision of the Examining Division 067 of the European Patent Office of 01.03.82. That decision was based on claims 1-3 as submitted on 02.05.81.

II. The reason given for the refusal was that the subject-matter of the claims did not involve an inventive step having regard to US-A-3 993 919 and Hsu, IBM Technical Disclosure Bulletin, August 1976, pages 998-999.

III. The appellant lodged an appeal against this decision on 21.04.82. The appeal fee was paid on the same date. The Statement of Grounds accompanied by an amended claim 1 was filed on 17.05.82.

IV. In a communication of 11.02.82 the Rapporteur of the Board of Appeal drew the appellant's attention to some further documents reflecting the state of the art, in the light of which the claims appeared to be unallowable.

V. In the Statement of Grounds, and during the oral proceedings which were held on 24.10.83 and in his letters of 26.02.83 and 31.10.83 the appellant argued essentially as follows: The teachings in US-A-3 993 919 and the article by Hsu do not indicate any need for an additional driver in a PLA. The US patent does not state what kind of load is to be driven by the off-chip driver (48) or that such kind of driver could be used between a decoder and an AND-array in a PLA. The article by Hsu discloses

a driver which is not suitable for use in a PLA, i.e. for driving high capacitive loads. The articles by Wood and Delahanty, cited by the Rapporteur, refer to dynamic PLA's and in the former the problem of driving high capacitive loads is not mentioned. The drivers are used as delay buffers.

A person skilled in the art starting from the Wood reference must seek information from Delahanty in order to be instructed about the capacitive load problem. Then he has to switch to the concept of a static PLA and find the Knepper reference (also cited by the Rapporteur) as the best solution for a driver circuit. The next step is to modify the Knepper circuit according to the Hsu reference neglecting, however, the purpose of the Hsu circuit, which is to drive non-capacitive loads. Such a succession of steps is typical for a patentable invention. The problem to be solved by the invention is to reduce the overall delay in a PLA caused by input and array capacitances, the driver circuit providing isolation between input and array. The design of a PLA is a difficult task and in the LSI and VLSI technology applied therein it is never obvious to change existing designs e.g. to leave out components.

VI. The appellant requested that a European patent be granted on the basis of the claims filed on 17.05.82. These claims read as follows:

1. A programmed logic array circuit including a prearray logic section (23), a search section (21) of AND type and read section (22) of OR type, arranged serially respectively between the array input and output (fig. 2,8), the prearray logic section including at least one

partitioning logic circuit block (30-39) wherein each logical input variable (A,B) is inverted and both the inverted value (A, B) and the value itself are combined to provide a separate logic output line for each of all logical combinations of the input signal variables (A, B) and their inverted values (A, B), characaterised in that each said logic output line is connected to the input (1) of a true push-pull driver circuit (36-39) in said block in the prearray section, said driver circuit including first (5) and second (6) field effect transistors connected, respectively, in series source-to-drain between a reference potential (4) of the driver circuit and a drive voltage (7), a driver output (2, 40-43) connected to the junction between said first and second transistors and driver input (1) connected to the gate (9) of the second transistor (6), and a third field effect transistor (11) applying the inversion of the driver input to the gate (16) of said first transistor (5), whereby no path exists between the drain of said second transistor (6) and the source of said first transistor (5), so that any d.c. power dissipation is eliminated in the output stage of the push-pull driver.

2. A logic array circuit of claim 1, wherein an isolation type circuitry is provided comprising an isolating field effect transistor (54) having its gate connected to reference potential and having its source connected to said search section (21) and its drain connected to said read section (22).

3. A logic array circuit of claim 1, wherein an isolating device (54a) is provided between an output line (61) of the read section (22) and an output device (62,63) for the logic array.

VII. As the composition of the Board had to be changed after oral proceedings had taken place but before a decision had been taken owing to the death of a member of the Board, the appellant was asked in a communication of 06.08.84 whether he wished to request new oral proceedings in accordance with Article 7 of the Rules of Procedure of the Boards of Appeal.

The appellant replied in a letter dated 16.08.84 that he did not desire new oral proceedings.

Reasons for the decision

1. The appeal complies with Articles 106-108 and Rule 64 EPC and is therefore admissible.

2. By reason of the facts and matters set out in paragraph VII above the Board is entitled to decide on the case in its present composition.

3. PLAs are generally known, both in dynamic and static form, although interest in development has centered on the first form in the past. Dynamic PLAs can be used to perform sequential logic because of the feedback introduced between blocks of combinational logic. Their operation is controlled by clock signals.

4. It is known (Wood, IBM Journal of Research and Development, Vol. 19, No. 4, July 1975, pages 379-383) to provide on a dynamic PLA-chip non-inverting buffer circuits in the form of bootstrap drivers between the two-bit partitioning device and the AND (Search) - section. These bootstrap drivers are clocked for dynamic to static interfacing and it is well known to the person skill-

ed in the art that they are capable of driving high fan-out. It being also well known that the AND-array presents a predominantly capacitive load, clearly the bootstrap drivers are provided to assure proper driving of this array, as is confirmed in the article by Delahanty, IBM Technical Disclosure Bulletin, Vol. 19, No.1, June 1976, pages 152-153. Similar bootstrap drivers are present between the AND-section and the OR-section and at the output of the OR-section.

5. According to the description, the application sets out to solve the problem of array capacitance and its effect on signal delay in a PLA, which problem is solved by the provision of the true (non-inverting) push-pull driver circuit disclosed in the application. This driver has the property of always presenting a path operating to charge or discharge the capacitance of the load being driven. Only one of the transistors in the series-connection is "on" at any time. It is stated on page 11 of the description that the use of such a driver results in a high performance low power static PLA.

6. It is evident that insofar as the high fan-in and fan-out circumstances in the AND- and OR- arrays are concerned there is in principle no difference between static and dynamic PLAs. Also the problems caused by the higher capacitance of larger arrays are the same.

7. It follows that to obtain small signal delays in the operation of a static PLA drivers have to be used having a high speed/power figure of merit. It is clear, however, that in a static PLA, where no clock signals are present, the introduction of delay between successive operation cycles is not required and the known bootstrap drivers cannot be used.

8. A buffer stage (inverting driver) having an inverter stage and a push-pull end stage comprising two series connected enhancement mode devices is known from an article cited by the applicant in IEEE Journal of Solid-State Circuits, April 1969, Vol. SC-4, No. 2, pages 57-64, Fig. 5C. According to the article this buffer stage has a high current drive capability in both on- and off-transitions. An identical buffer stage is used as an off chip output driver (48) in a dynamic PLA (US-A-3 993 919, published 1976) and in a push-pull logical circuit (Homan, IBM Technical Disclosure Bulletin, Vol. 18, no. 3, August 1975, pages 910-911). This article also shows the use of a depletion-mode FET in the inverter stage preceding the push-pull end stage and mentions an improvement over prior art arrangements of 2:1 in the speed/power figure of merit. It follows from the known properties of enhancement mode devices that in these known driver circuits no path exists between the drain of the upper transistor in the series connection and the source of the lower transistor.

9. Furthermore, Knepper, IBM Technical Disclosure Bulletin, Vol. 19, no. 3, August 1976, pages 922-923 discloses the use of the same push-pull arrangement of enhancement mode devices in an inverting and a non-inverting driver and it is stated that such drivers are particularly useful when driving large fan-out and high capacity.

10. As drivers having a push-pull end state comprising two series connected enhancement mode devices are clearly particularly advantageous so far as their speed/power merit figure is concerned, the use of such a driver in a static PLA between the pre array logic section and the AND-array appears to be an obvious choice.

11. It is known (see paragraph 2 above) that the driver between the pre array logic section and the AND-array has to be non-inverting. The non-inverting driver disclosed in the present application cannot be considered as involving an inventive step as the only change to be made to the drivers known (paragraph 7 above) is to interchange the connections to the upper and lower transistors in the series connection. This is also known in itself, see the article by Knepper and the article Hsu, IBM Technical Disclosure Bulletin, vol. 19, no. 3, August 1976, pages 998-999.

12. It follows that the alleged problem of array capacitance could readily be solved by reference to the available technical literature and the exercise of routine design skill in choosing appropriate circuit elements taking into account their known and obviously relevant characteristics and obtaining a result which is in no way unexpected. Under these circumstances the Board of Appeal is of the opinion that claim 1 does not involve an inventive step and is, therefore, unallowable.

13. Isolation circuits as mentioned in claim 2 are known per se from Electronics, 19 February 1976, page 115 and from the article by Blaser and Conrad, IEEE International Solid-State Circuits Conference, 15 February 1978, pages 14-15, cited in the present application. The use of such isolation circuitry between the search and the read section of a PLA is considered to be obvious to a person skilled in the art. In the combination with the push-pull driver circuit mentioned in the characterising part of claim 1, both circuits operate independently of each other and no unexpected effect is present.

The same reasoning applies, mutatis mutandis, to claim 3. Neither claim, therefore, is considered to be allowable.

Order

For these reasons, it is decided that:

The appeal is dismissed.