Unified Patent Court
Einheitliches Patentgericht
Juridiction unifiée du brevet

Decision

of the Court of First Instance of the Unified Patent Court
Local Division Munich
delivered on 11 March 2026

HEADNOTES

The "attacked embodiment" is regularly determined by the factual design of a certain product or a process with regard to the features of the invoked patent claim as asserted in the Statement of Claim. This can be a specific product determined, for example, by its product name, product sheet and technical design. However, the attacked embodiment may also comprise all products that generally have the technical features specified by the Claimant, which allegedly realise the technical teaching of the patent claim. This may also include products unknown to the Claimant or, in the case of an injunction, future products insofar as they essentially correspond to the features of the product presented by the Claimant in his Statement of Claim, which he considers decisive for the patent infringement. In such a case, it is usually sufficient if the Claimant has exemplified the infringement on a sample of the attacked embodiment.

Network System Technologies LLC, legally represented by its Chief Executive Officer (CEO) Warren Hurwitz,533 Congress Street, Portland, ME 04101, United States of America,

represented by:	Dr. Thomas Gniadek, Hoffmann Eitle Patent- und Rechtsanwälte PartmbB, Arabellastraße 30, 81675 Munich.

DEFENDANTS AND COUNTERCLAIMANTS

3. **Qualcomm Incorporated**, legally represented by its Chief Executive Officer (CEO) Cristiano Amon, 5775 Morehouse Drive, San Diego, CA 92121, United States of America,

4. **Qualcomm Technologies, Inc.**, legally represented by its Chief Executive Officer (CEO) Cristiano Amon, 5775 Morehouse Drive, San Diego, CA 92121, United States of America,

5. **Qualcomm Germany GmbH**, legally represented by its Chief Executive Officer (CEO) Hamid-Reza Nazeman, Anzinger Straße 13, 81671 Munich, Germany,

represented by:	Johannes Heselberger, Bardehle Pagenberg Partnerschaft mbB, Prinzregentenplatz 7, 81075 Munich.

PATENT AT ISSUE

European Patent n° EP 1 552 669

PANEL/DIVISION

Panel 2 of the Local Division Munich

DECIDING JUDGE/S

This decision has been issued by Presiding Judge U. Voß, legally qualified Judge D. Voß (Judge-rapporteur), legally qualified Judge P. Perrotti and technically qualified Judge A. Scilletta

LANGUAGE OF THE PROCEEDINGS

English

SUBJECT-MATTER OF THE PROCEEDINGS

Infringement action and Counterclaim for revocation

16 December 2025

1   The subject matter of these proceedings is an Infringement action brought by the Claimant against the Defendants 3) to 5) and a Counterclaim for revocation brought by the Defendants 3) to 5) (hereinafter: Defendants). The proceedings are part of an international patent dispute between the Claimant and the Defendants. Claimant has also filed a U.S. civil action in the United States District Court for the Western District of Texas (Austin Division), Civil Action No. 1:22-cv-1331 against the Defendants 3) and 4) and Arteris, Inc.

2   Originally, the Claimant also sued Samsung Electronics Co., Ltd. and Samsung Semiconductor Europe GmbH (Defendants 1) and 2)), two companies belonging to the Samsung Group, which also filed a Counterclaim for revocation. On 6 September 2024, at request of the Claimant and the Defendants 1) and 2), the Court permitted the withdrawal of the Infringement action and the Counterclaim for revocation in relation to Defendants 1) and 2) respectively.

3   The basis for the present Infringement action and the object of the related Counterclaim for revocation is the European Patent EP 1 552 669 (Exhibit P 1; hereinafter: patent-in-suit) regarding an integrated circuit and a method for establishing transactions. The application of the patent-in-suit was filed by Koninklijke Philips Electronics N.V. on 4 July 2003, claiming priority of the European application No. 02079196 dated 8 October 2002. The patent application was published on 13 July 2005, the mention of the grant of the patent-in-suit on 19 September 2007. The patent-in-suit was validated in a number of jurisdictions including France, Germany and the United Kingdom, where it remained in force until the patent term expired on 4 July 2023. The patent-in-suit was opted out of the competence of the UPC on 25 May 2023, but this opt-out was subsequently withdrawn on 20 December 2023. A preliminary objection based on the allegedly invalid withdrawal of the opt-out was rejected by order dated 25 August 2025.

4   Claimant asserts claim 1 of the patent-in-suit which reads as follows:

> Integrated circuit comprising a plurality of modules (M, S), and a network (N) arranged for transferring messages between said modules (M, S), wherein a message issued by a first module (M) comprises first information indicative for a location of an addressed module within the network, and second information indicative for a location within the addressed module (S),

at least one network interface means (ANIP, PNIP) coupled between one of the modules (M, S) and the network (N) for managing the communication between said associated module (M, S) and the network (N), **characterized by**

at least one address translation means (AT) arranged in one of said interface means (ANIP, PNIP) for arranging the first and the second information as a single address,

wherein said address translation means (AT) is adapted to determine which module is addressed based on said single address, and

wherein the network interface determines the selected location of the addressed module (S) based on said single address.

5   With regard to the dependent claims 2, 3 and 4 of the patent-in-suit, the infringement of which is alternatively asserted by the Claimant, it is referred to the patent specification (Exhibit P 1).

6   Originally, the actual and registered proprietor of the patent-in-suit was Koninklijke Philips Electronics N.V. (hereinafter: "Philips"). On 24 June 2022, the Claimant and Philips concluded a Patent Purchase Agreement (PPA) according to which the patent-in-suit and an associated integrated circuits patent portfolio should be transferred from Philips to the Claimant. Corresponding Patent Assignments ("PAs") covering the French and the German Part of the patent-in-suit were signed on 5 July 2022 The transfer and change of ownership, the effectiveness of which is disputed by the Defendants, were recorded in the EPO patent register on 8 May 2023 as well as in the national patent registers of France and Germany. An excerpt of these registers have been submitted as Exhibit P 2 – P 5.

7   The Claimant is a patent licensing company that seeks to license the patent-in-suit and the corresponding patent portfolio to semiconductor companies and companies that deploy those semiconductors.

8   Defendant 3) creates and designs semiconductors, software and services related to wireless technology.

9   Defendant 4) is a subsidiary of Defendant 3) and operates, along with its subsidiaries, substantially all of Qualcomm's engineering, research and development functions, and substantially all of their products and services businesses, including the QCT semiconductor business. The product range of Defendant 4) includes, among other things, Snapdragon and Qualcomm branded products.

10   Defendant 5) is a subsidiary of Defendant 3) and Defendant 4).

11   Defendant 3) and Defendant 4) design a variety of products regarding wireless technology, including ICs and especially the Snapdragon SoC family, which is used, for example, in smartphones, laptops, VR devices, automotive etc.

12 Arteris, Inc. is a technology firm developing, inter alia, NoC technology (hereinafter: Arteris). According to an Arteris, Inc. press release and other news sources from 2013, Defendant 4) hired approximately 43 Arteris engineers and acquired certain Arteris SoC technology and IP in 2013, licensed such SoC technology and IP back to Arteris, and provided improvements to, and engineering support for, such SoC technology and IP to Arteris.

13 The Claimant is objecting to integrated circuits (ICs) offered and distributed by the Defendants 3) to 5). These ICs including Systems on Chip (SoCs), have Network on Chip (NoC) interconnects (hereinafter: Qualcomm NoC ICs), i.e. they comprise a network as on-chip interconnect. According to the Claimant's submission, these NoCs include (but are not limited to) a NoC designed using tools developed by Arteris and/or derivatives thereof (hereinafter: Arteris NoC). For the further explanation of the Arteris NoC, the Claimant refers to Chapter 11 of the book titled 'Networks-on-Chips Theory and Practice' (submitted as Exhibit P 11; hereinafter: Arteris NoC Chapter).

14 According to the Arteris NoC Chapter, the Arteris NoC is a network on board of the IC which allows the modules of the IC, also referred to as functional blocks, IP blocks or nodes, to communicate with each other. Network interface units (NIUs) and routers/switches are key components of the Arteris NoC, which also makes use of a specific network protocol called NoC Transaction and Transport Protocol (NTTP) proposed by Arteris. This protocol is packet based and adopts a three-layered approach with transaction, transport and physical layers. It defines the rules and conventions that apply as data is transferred over the network. Requests from a (master) module are sent through the master NIU to the NoC from which they are routed to the NIU of a (slave) module. Response packets from the (slave) module are delivered vice versa through the slave NIU via the network to the requesting master NIU which forwards them to the (master) module. The NIUs create the packets. They translate between third-party protocols like AHB, OCP and AXI used by the modules and the NTTP protocol. For further details of the Arteris NoC, reference is made to the Arteris NoC chapter (Exhibit P 11).

15 The Claimant refers to Qualcomm NoC ICs that include Arteris NoC as "infringing embodiment II" (whereas the term infringing embodiment I is referred to products of Samsung). The following products of the Defendants 3) and 4) are examples of the infringing embodiments II:

16 The Snapdragon Mobile Processors, Platforms and Modems, including:

• Snapdragon 8 Gen 3	• Snapdragon S4 Pro	• Snapdragon 865
• Snapdragon 8 Gen 2	• Snapdragon S4 Plus	• Snapdragon 860
• Snapdragon 8+ Gen 1	• Snapdragon S4 Prime	• Snapdragon 855+
• Snapdragon 8 Gen 1	• Snapdragon S3	• Snapdragon 855
• Snapdragon 7+ Gen 2	• Snapdragon S2	• Snapdragon 845
• Snapdragon 7 Gen 1	• Snapdragon S1	• Snapdragon 835
• Snapdragon 6 Gen 1	• Snapdragon 888+	• Snapdragon 821
• Snapdragon 4 Gen 2	• Snapdragon 888	• Snapdragon 820
• Snapdragon 4 Gen 1	• Snapdragon 870	• Snapdragon 810
• Snapdragon S4 Play	• Snapdragon 865+	• Snapdragon 808

- Snapdragon 805
- Snapdragon 801
- Snapdragon 800
- Snapdragon 782G
- Snapdragon 782
- Snapdragon 780G
- Snapdragon 780
- Snapdragon 778G+
- Snapdragon 778G
- Snapdragon 768G
- Snapdragon 768
- Snapdragon 765G
- Snapdragon 765
- Snapdragon 750G
- Snapdragon 750
- Snapdragon 732G
- Snapdragon 732
- Snapdragon 730G
- Snapdragon 730
- Snapdragon 720G
- Snapdragon 720
- Snapdragon 712
- Snapdragon 710
- Snapdragon 695
- Snapdragon 690
- Snapdragon 685
- Snapdragon 680
- Snapdragon 678
- Snapdragon 675
- Snapdragon 670
- Snapdragon 665
- Snapdragon 662

- Snapdragon 660
- Snapdragon 652
- Snapdragon 650
- Snapdragon 636
- Snapdragon 632
- Snapdragon 630
- Snapdragon 626
- Snapdragon 625
- Snapdragon 617
- Snapdragon 616
- Snapdragon 615
- Snapdragon 610
- Snapdragon 600
- Snapdragon 480+
- Snapdragon 480
- Snapdragon 460
- Snapdragon 450
- Snapdragon 439
- Snapdragon 435
- Snapdragon 430
- Snapdragon 429
- Snapdragon 427
- Snapdragon 425
- Snapdragon 415
- Snapdragon 412
- Snapdragon 410
- Snapdragon 400
- Snapdragon 215
- Snapdragon 212
- Snapdragon 210
- Snapdragon 208
- Snapdragon 200

- Snapdragon X75
- Snapdragon X72
- Snapdragon X70
- Snapdragon X65
- Snapdragon X60
- Snapdragon X55
- Snapdragon X50
- Snapdragon X35
- Snapdragon X20
- Snapdragon X24
- Snapdragon X16
- Snapdragon X15
- Snapdragon X12
- Snapdragon X7
- Snapdragon X5
- MDM9625
- MDM9615
- MDM9225
- MDM9215
- MDM9600
- MDM8225
- MDM9200
- MDM9207-1
- MDM9206
- MDM8215
- MDM8220
- MDM6600
- MDM8200A
- MDM6270
- MDM6200
- 9205

17 The Snapdragon Mobile Compute Processors, including:

- Snapdragon 835 Mobile PC Platform
- Snapdragon 850 Mobile PC Platform
- Snapdragon 7c Compute Platform
- Snapdragon 7c Gen 2 Compute Platform
- Snapdragon 7c+ Gen 3 Compute Platform

- Snapdragon 8c Compute Platform
- Snapdragon 8cx Compute Platform
- Snapdragon 8cx Gen 2 5G Compute Platform
- Snapdragon 8cx Gen 3 Compute Platform

18 The Snapdragon Wearable Processor, including:

- Snapdragon Wear 1100
- Snapdragon Wear 1200
- Snapdragon Wear 2100

- Snapdragon Wear 2500
- Snapdragon Wear 3100
- Snapdragon Wear 4100

- Snapdragon Wear 4100+
- Snapdragon W5
- Snapdragon W5+ Gen 1

19 The Snapdragon Automotive Processors, including:
   • Snapdragon 602A   • Snapdragon 820A   • Snapdragon 855A

20 The Snapdragon Embedded Processors, including:
   • Snapdragon 410E   • Snapdragon 800   • Snapdragon 820E
   • Snapdragon 600E   • Snapdragon 810

21 The Qualcomm Vision Intelligence Processors, including:
   • QSC603   • QSC605

22 The Qualcomm Home Hub and Smart Audio Processors, including:
   • APQ8009   • QSC403   • QSC407
   • APQ8017   • QSC404
   • APQ8053   • QSC405

23 The Qualcomm Extended Reality (XR) Processors, including:
   • Snapdragon XR1   • Snapdragon XR2

24 The Qualcomm Gaming Processors, including:
   • Snapdragon G3x Gen 1

25 Other Qualcomm Processors, including:
   • QSC1100   • MSM6125   • MSM6550
   • QSC6010   • MSM6150   • MSM6550A
   • QSC6020   • MSM6175   • MSM6800
   • QSC6030   • MSM6000   • MSM6500
   • QSC6240   • MSM6225   • MSM7200
   • QSC6245-1   • MSM6250   • MSM7200A
   • QSC6055   • MSM6250A   • MSM7201
   • QSC6065   • MSM6245   • MSM7500
   • QSC6260-1   • MSM6255   • MSM7500A
   • QSC6270   • MSM6260   • MSM7600
   • QSC6075   • MSM6275   • MSM7850
   • QSC6085   • MSM6280   • Qualcomm 205
   • MSM6025   • MSM6280A   • Qualcomm 215
   • MSM6050   • MSM6800A
   • MSM6100   • MSM6575

26 The Claimant also objects to Samsung Galaxy smartphones, chromebooks, laptops and
   tablets which contain various models of the "infringing embodiments II" and are offered,
   imported and sold throughout Europe, inter alia in Germany and France, by the former
   Defendants 1) and 2). The Claimant designates these products as "infringing embodiment IV"
   (whereas the term infringing embodiment III referred to products of Samsung containing the

infringing embodiment I) and lists the following products as examples for the "infringing embodiment IV":

27 Samsung Galaxy S-Series smartphones:
- Samsung Galaxy S23 Ultra
- Samsung Galaxy S23 Plus
- Samsung Galaxy S23
- Samsung Galaxy S22 Ultra 5G
- Samsung Galaxy S22 Ultra
- Samsung Galaxy S22 Plus
- Samsung Galaxy S22 5G
- Samsung Galaxy S22+ 5G
- Samsung Galaxy S22
- Samsung Galaxy S21 Ultra 5G
- Samsung Galaxy S21+
- Samsung Galaxy S21+ 5G
- Samsung Galaxy S21 5G
- Samsung Galaxy S21 Fan Edition 5G
- Samsung Galaxy S20 Ultra 5G
- Samsung Galaxy S20 Ultra
- Samsung Galaxy S20+ 5G
- Samsung Galaxy S20 5G
- Samsung Galaxy S20 FE 5G
- Samsung Galaxy S20 FE
- Samsung Galaxy S20+
- Samsung Galaxy S20
- Samsung Galaxy S10 5G
- Samsung Galaxy S10+
- Samsung Galaxy S10e
- Samsung Galaxy S10 Lite
- Samsung Galaxy S10
- Samsung Galaxy S9+
- Samsung Galaxy S9
- Samsung Galaxy S8+
- Samsung Galaxy S8 Active
- Samsung Galaxy S8
- Samsung Galaxy S7 Edge
- Samsung Galaxy S7 Active
- Samsung Galaxy S7
- Samsung Galaxy S Light Luxury

28 Samsung Galaxy A-Series smartphones:
- Samsung Galaxy A90 5G
- Samsung Galaxy A80
- Samsung Galaxy A73 5G
- Samsung Galaxy A72
- Samsung Galaxy A71 5G
- Samsung Galaxy A71
- Samsung Galaxy A70s
- Samsung Galaxy A70
- Samsung Galaxy A60
- Samsung Galaxy A52s 5G
- Samsung Galaxy A52 5G
- Samsung Galaxy A52
- Samsung Galaxy A51 5G
- Samsung Galaxy A42
- Samsung Galaxy A23 5G
- Samsung Galaxy A23
- Samsung Galaxy A20s
- Samsung Galaxy A11
- Samsung Galaxy A9 Pro
- Samsung Galaxy A9
- Samsung Galaxy A8 Star
- Samsung Galaxy A8s
- Samsung Galaxy A6+
- Samsung Galaxy A6s
- Samsung Galaxy A02s
- Samsung Galaxy A01

29 Samsung Galaxy M-Series smartphones:
- Samsung Galaxy M52 5G
- Samsung Galaxy M51
- Samsung Galaxy M42 5G
- Samsung Galaxy M40
- Samsung Galaxy M23
- Samsung Galaxy M11
- Samsung Galaxy M02s
- Samsung Galaxy M01

30 Samsung Galaxy J-Series smartphones:
- Samsung Galaxy J8
- Samsung Galaxy J7 V
- Samsung Galaxy J6+
- Samsung Galaxy J4+
- Samsung Galaxy J4 Core
- Samsung Galaxy J3
- Samsung Galaxy J2 Pro
- Samsung Galaxy J2 Core

31 Samsung Galaxy Note-Series smartphones:
- Samsung Galaxy Note20 Ultra 5G
- Samsung Galaxy Note20 Ultra
- Samsung Galaxy Note20 5G
- Samsung Galaxy Note20
- Samsung Galaxy Note10+ 5G
- Samsung Galaxy Note10+
- Samsung Galaxy Note10 5G
- Samsung Galaxy Note10
- Samsung Galaxy Note9
- Samsung Galaxy Note8
- Samsung Galaxy Note7

32 Samsung Galaxy F-Series smartphones:
- Samsung Galaxy F52 5G
- Samsung Galaxy F23
- Samsung Galaxy F02s

33 Samsung Galaxy Z-Series smartphones:
- Samsung Galaxy Z Flip5
- Samsung Galaxy Z Flip4
- Samsung Galaxy Z Flip3 5G
- Samsung Galaxy Z Flip 5G
- Samsung Galaxy Z Flip
- Samsung Galaxy Z Fold 4
- Samsung Galaxy Z Fold3 5G
- Samsung Galaxy Z Fold2 5G

34 Samsung Galaxy Fold/Folder-Series smartphones:
- Samsung Galaxy Fold 5G
- Samsung Galaxy Fold
- Samsung Galaxy Folder2

35 Other Samsung Galaxy smartphones:
- Samsung Galaxy C7
- Samsung Galaxy Quantum 2
- Samsung Galaxy On7
- Samsung Galaxy Xcover6

36 Samsung Galaxy Book Chromebooks and Laptops:
- Samsung Galaxy Book Go 5G
- Samsung Galaxy Book Go
- Samsung Galaxy Book S LTE

37 Samsung Galaxy Tab-Series Tablets:
- Samsung Galaxy Tab S9 Ultra
- Samsung Galaxy Tab S8+
- Samsung Galaxy Tab S7 FE
- Samsung Galaxy Tab S7
- Samsung Galaxy Tab S6 Lite
- Samsung Galaxy Tab S5e
- Samsung Galaxy Tab S3 9.7
- Samsung Galaxy Tab S2 8.0
- Samsung Galaxy Tab A 8.0
- Samsung Galaxy Tab Active4 Pro
- Samsung Galaxy Tab S8 Ultra
- Samsung Galaxy Tab S8
- Samsung Galaxy Tab S7+
- Samsung Galaxy Tab S6 5G

- Samsung Galaxy Tab S6
- Samsung Galaxy Tab S4 10.5
- Samsung Galaxy Tab S2 9.7

- Samsung Galaxy Tab A7 10.4
- Samsung Galaxy Tab A 10.5
- Samsung Galaxy Tab Active Pro

REQUESTS

38 In the infringement action, the Claimant originally requested, among other things, that the Defendants held liable for all damages resulting from the infringement of claim 1 of the patent-in-suit since 19 October 2007 until 4 July 2023 in the territories of the French Republic, the Federal Republic of Germany and the United Kingdom of Great Britain and Northern Ireland.

39 After the Court has allowed the Claimant to unconditionally limit the claim to the territories of France and Germany, the Claimant still requests:

I. The Defendants are ordered,

1. with regard to products in the territories of the French Republic and/or the Federal Republic of Germany comprising an

integrated circuit comprising

a plurality of modules, and a network arranged for transferring messages between said modules,

wherein a message issued by a first module comprises first information indicative for a location of an addressed module within the network, and second information indicative for a location within the addressed module,

at least one network interface means coupled between one of the modules and the network for managing the communication between said associated module and the network, characterized by

at least one address translation means arranged in one of said interface means for arranging the first and the second information as a single address,

wherein said address translation means is adapted to determine which module is addressed based on said single address, and wherein the network interface determines the selected location of the addressed module based on said single address

(direct infringement of claim 1),

alternatively and in particular if

said address translation means is arranged in said interface means associated to said first module

(direct infringement of dependent claim 2),

alternatively and in particular if

said address translation means comprises an address mapping table

(direct infringement of dependent claim 3),

alternatively and in particular if

said address mapping table contains fields for every channel of a connection, for network interface ports of a connection, and for local addresses in addressed modules

(direct infringement of dependent claim 4),

which have been put on the market since the date of publication and mention of the grant of EP 1 552 669 B1 on 19 September 2007 until its expiry on 4 July 2023, at their own expense, to

a. recall the aforesaid products from the channel of commerce by requesting in writing the respective commercial customers in possession of the infringing products to return them to the Defendants, with reference to the fact that in the judgement to be designated the court addressed has found an infringement of the European Patent EP 1 552 669 B1, whereby the commercial customers are promised that in the event that the infringing products are returned, they will be refunded the purchase price already paid, if any, as well as the transport or shipping costs incurred as a result of the return, including any customs and storage costs,

b. definitely remove the aforesaid products from the channel of commerce by taking back the recalled products, and

c. hand over the aforesaid products in their direct or indirect possession or ownership to a bailiff to be appointed by the Plaintiff for destruction at the Defendants' expense or, at their option, to destroy the aforesaid products themselves or, at their option, to deprive the aforesaid products of its infringing property by removing and destroying the inbuilt infringing means;

2. to inform the Plaintiff of

a. the origin and distribution channels of the products referred to in section I.1. which have been put on the market since 19 October 2007 until 4 July 2023,

b. the quantities produced, manufactured, delivered, received or ordered, as well as the price obtained for the products referred to in section I.1. which have been put on the market since 19 October 2007 until 4 July 2023, and

c. the identity of any third person involved in the production or distribution of the products referred to in section I.1 which have been put on the market since 19 October 2007 until 4 July 2023;

3. to pay to Plaintiff an interim award of damages in an amount at the discretion of the Court.

II. Each individual failure to comply with any order pursuant to sections I.1. to I.3. will render the respective Defendant liable to pay to the Court a possibly repeated penalty of up to EUR 250,000.00 per day for each day the respective Defendant fails to comply.

III. The Defendants are liable for all damages resulting from the patent infringement as specified under section I.1. since 19 October 2007 until 4 July 2023 in the territories of the French Republic and the Federal Republic of Germany.

IV. The Plaintiff is permitted, at Defendants' expense, to display the decision and publish it in full or in part in a daily newspaper with nationwide circulation in each of the territories referred to in section I.1.

V. The Defendants 3) to 5) are ordered to bear the costs jointly and severally.

VI. The aforesaid orders are immediately enforceable. In the event that a security is ordered, the Plaintiff is permitted to provide security by bank or savings bank guarantee. The amount of the security shall be determined separately for each enforceable order, and we consider the following partial security to be appropriate:

Section I.1.a, I.1.b (recall and removal): 50 % of the total security

Section I.1.c (destruction): 30 % of the total security

Section I.2 (information): 10 % of the total security

Section I.3 (interim damages): 7.5 % of the total security

Section IV (notice of judgment): 2.5 % of the total security.

40 The Defendants request in the infringement action:

I. The complaint is rejected.

II. Claimant is ordered to pay the costs of the proceedings.

III. Claimant is ordered to provisionally reimburse the costs of Defendants 3) to 5).

Alternatively:

IV. The enforcement of the decision is subject to an appropriate security to be determined by the Court and to be provided by Claimant.

V. The decision, including the orders contained therein, is made subject to the condition precedent that the patent-in-suit is not held to be wholly or partially invalid by the final decision – alternatively a first instance decision – in (other) revocation actions, including counterclaims for revocation.

Auxiliary:

The decision, including the orders contained therein, is made subject to the condition subsequent that the patent-in-suit is held to be wholly or partially invalid by the first instance decision – alternatively the final decision – in (other) revocation actions, including counterclaims for revocation.

41 The Claimant requests,

to reject Defendants' 3), 4) and 5) requests under III., IV. and V.

42 For the Counterclaim for revocation, the Defendants request:

I. European Patent 1 552 669 B1 is revoked in its entirety for the territory of Germany and France.

II. Claimant is ordered to pay the costs of the proceedings regarding the counterclaim for revocation.

III. Claimant is ordered to provisionally reimburse the costs of Defendants 3) to 5).

43 The Claimant requests in the Counterclaim for revocation:

I. The counterclaims for revocation of the Defendants 3), 4) and 5) are rejected.

in the alternative:

The patent EP 1 552 669 B1 is upheld to the extent of the auxiliary requests 1 to 4 in this numerical order as submitted in Exhibit AR 1, 2, 3a and 4a, and the Counterclaim is dismissed in all other respects [*cf. audio recording of the oral hearing*].

II. Defendants 3), 4) and 5)'s request that the Claimant is ordered to provisionally reimburse the costs of the Defendant is rejected.

III. Defendants 3), 4) and 5) are ordered to jointly pay the costs of the proceedings regarding the counterclaims for revocation.

44 During the oral hearing, the Claimant set out that the patent-in-suit can always be revoked in part based on all pending auxiliary requests as the independent claim 5 does not suffer from any potential extension beyond the original disclosure. If no auxiliary request remedies the alleged inadmissible extension of claim 1, at least claim 5 can be maintained. According to the Claimant, this is applicable to all (auxiliary) requests.

POINTS AT ISSUE

Standing to sue

45 The Claimant consider himself to have standing to sue. Claimant and Philips are in agreement that the patent-in-suit and its annex claims have been transferred effectively. A third party as the Defendants cannot challenge that. Against this background, the Claimant has standing to sue unless the Defendants can prove otherwise by substantially disputing facts which they did not. Furthermore, the entry in the respective patent register provides the (refutable) assumption that the registered individual/company is the actual proprietor, which is the case here. This cannot be eliminated by simply disputing. Finally, as a mere precaution, the Claimant relies on the PPA and PAs submitted as Exhibits P 24 and P 25, which, according to the Claimant, show that the patent-in-suit and all claims have been effectively transferred. The Claimant particularly states that the signatories of the agreements were duly authorised as confirmed by several witness statements.

46 The Defendants are of the opinion that the Claimant does not have standing to sue for the asserted claims. The Claimant has neither shown that it has validly acquired the patent-in-suit, nor that the claims for the past have been validly assigned to the Claimant. In clear contradiction to the front-loaded system, the Claimant did not provide any evidence in its Statement of claim of an effective assignment of claims for the period before the (alleged) acquisition of the patent-in-suit, nor did the Claimant provide any evidence for the effectiveness of the alleged transfer of the patent-in-suit. The burden of proof for the effective patent assignment lies with the Claimant.

47 Insofar as the Claimant has submitted a PPA and corresponding PA, the Defendants argue that these documents have been late-filed and must not be considered. Notwithstanding this, the Defendants dispute, based on different colours and formats of single pages of the PPA, which are also partly tilted, that Exhibit P 24 is a true copy of the original PPA (ink version), as signed by the parties to the PPA, including the exhibits thereto, in particular Exhibit A to the PPA. They also dispute that the patent-in-suit is listed in the original PPA (ink version), as signed by the parties to the PPA.

48 The Defendants further dispute that the conditions in sec. 4.1 PPA were fulfilled, in particular that the purchase price was received by Philips in full at the Closing and that the assignment of the patent-in-suit was unhindered by the Encumbrances, Identified Agreements and Current Agreements. The Defendants dispute that sec. 4.1 PPA covers the asserted claims and they dispute, in particular, that it was Claimant's and Philips' intention to assign such claims with the PPA. The Defendants further dispute that the asserted claims under the patent-in-suit were validly acquired by the Claimant by means of the PAs. They dispute that it was Claimant's and Philips' intention to assign the patent-in-suit with the PAs (anew) and that the PAs were correct in the sense that the assignment happened by means of the PPA before. Finally, the Defendants dispute that the signatories to the PPA and the PA had the authority to sign.

Claim construction

49 The Claimant is of the opinion that the term "integrated circuit" is used in the patent-in-suit under its normal meaning in the art, i.e. meaning a circuitry on a chip. An integrated circuit (IC) is an assembly of electric components such as transistors, resistors and capacitors, interconnected on a semiconductor material. ICs are also called chips or microchips. Systems on chip (SoCs) are embodiments of an IC. Hence, the skilled person would understand that SoCs are ICs according to claim 1. The IC within the claimed technical teaching comprises a network. According to the patent-in-suit, the network relates to a network-on-chip (NoC). Furthermore, an IC according to the invention comprises modules. These modules refer to (conventional) modules or functional blocks of an IC under their normal meaning in the art. A module performs a specific function in the overall operation of the IC and can for example be a computational element or a memory. An "intellectual property block (IP block), i.e. a predesigned module, may also be a module.

50 The Claimant further explains that according to the wording of claim 1, a message is issued by a first module comprising first information indicative for a location of an addressed module within the network and second information indicative for a location within the addressed module. According to the Claimant, the skilled person would understand that this "first information" and "second information" relate to addressing information that tell the recipient of the message where the message is addressed to. The patent-in-suit does not limit the first and second information to any particular type of information. The first and second information comprised in the issued message does not need to be two separate, i.e. distinct, pieces of information. The first information and second information may even exist as a single address until they are put together by the address translation means. The Claimant is of the opinion that the claim wording does not provide any requirements as to how the first information and the second information are arranged in the message. Even one item in one single address could be regarded as first and as second information at the same time. Moreover, it follows from the term "indicative" that it is sufficient if the network interface or network translation means can derive the specific location of the addressed module and the specific location within the addressed module from the respective first and second information.

51   The Claimant states that a network interface means according to claim 1 serves to manage communication between the module and the network. As the patent-in-suit explains, the network interface means allows that the module can perform its dedicated operation, without having to deal with communication with the network or other modules.

52   The Claimant then refers to the address translation means which, according to claim 1, is arranged in the network interface means. The Claimant is of the opinion that the "address translation means" refers to means within the IC that perform an address translation. The skilled person would understand from the wording of claim 1 that the address translation is performed by arranging the first and the second information as a single address. However, "for arranging" in the wording of the claim does not mean an active process in the sense that two distinct pieces of information must be put into a single address. It is rather sufficient that first and second information which were only received as "indicators" are processed by the network translation means. The claim wording leaves it open how and to which extend the "arranging" is done. According to the Claimant, the address translation typically involves mapping by means of a mapping table as in a preferred embodiment of the patent-in-suit.

53   Finally, claim 1 requires that the address translation means or the network interface respectively determine the addressed module and the location of the addressed module based on the single address. In the Claimant's view, this means that, based on the single address, it is possible to determine the destination of the message, i.e., which module is addressed and the selected location of the addressed module. Accordingly, the patent-in-suit describes that the first module can be implemented independent of the addressing to the addressed module, which is performed by the address translation means in one of the network interfaces. Therefore, the teaching of the patent-in-suit is to hide the addressing of data from the module. According to the object of the invention not to introduce too much data into the network, the design of the first module can be implemented independent of the address mapping to the addressed modules. The address mapping is handled by the network interface means. With regard to the claim wording "within the network", the Claimant is of the opinion that this does not require that the module is within the network but that this relates to the network interface associated to the addressed module. This network interface has an address within the network in order to ensure the communication with the network.

54   The Defendants point out that the patent-in-suit does not contain a definition of the term integrated circuit. Usually, an integrated circuit means a chip, i.e. a multiplicity of components, such as transistors, resistors, and capacitors, arranged and interconnected on a substrate of semiconductor material. The integrated circuit, here, comprises processing modules and a network. In the Defendants' view, a network need not to be a network on chip with connected nodes. Claim 1 does not limit the claimed network to a particular type of network. Rather, the patent-in-suit mentions different types of networks comprising buses, switches, and point-to-point wires.

55   The Defendants further explain that the modules within the meaning of claim 1 can be "computation elements" that interact with the network via network interfaces. The (first) module

issues messages which shall comprise both the first information indicative for a location of an addressed module and the second information indicative for a location within the addressed module. The Defendants are of the opinion that, at the time the message is issued, the first module must know both the location of the addressed module within the network and the target location within the addressed module, which are represented by the first and second information respectively. Therefore, the message must actually comprise two separate pieces of information. It would not be sufficient if the message issued by the first module contains only one integral information, such as one address which indicates the two claimed locations. Hence, claim 1 is limited to a situation in which the separate first information and second information do not exist as a single address until they are put together in that way by the address translation means. In the Defendants' view, the two locations have to be understood in connection with the network interface means, which are coupled between the modules and the network, meaning that the modules are outside the network. In this regard, the location of the addressed module "within the network", indicated by the first information, is not the location of the addressed module outside the network, but the location within the network via which the addressed module may be reached. Claim 1 does therefore not require a first information indicative for a location of an addressed module in global terms, but in relation to the network.

56 The Defendants argue that the network interface means are required to manage communication between the modules and the network because the modules are not part of the network. Therefore, the network interface means are coupled between one of the modules and the network, i.e. it neither belongs to a module nor to the network. Furthermore, the network interface means contain address translation means. The Defendants point out that neither the claim nor the description specify what the term "translation" shall mean. The only characterisation of the address translation means is its function of arranging first and second information as a single address. The Defendants are of the opinion that the word "arrange" means to combine, to order, to group, to assemble, to adapt, and so on, but does not cover mere data processing of the received information. In any event, an active processing of the two pieces of information must be performed. Hence, a person skilled in the art would understand that two separate pieces of information, which are received from a first module in a message, are now encoded into a single address, wherein this single address is then used for communication within the network. Memory mapping or address translation in general is not required.

57 Finally, the network interface and the address translation means arranged in the network interface means, respectively, are adapted to carry out two determining steps based on the single address. However, as the Defendants point out, they do not simply regain the first and second information for delivering the message issued by the first module. Rather, the addressed module ("which") and the location of the addressed module ("where") must be determined.

Validity

58 The Defendants are of the opinion that the patent-in-suit is to be revoked since the subject-matter of the independent claims extends beyond the content of the application as originally

filed. During the examination proceedings, the applicant asserted that the new claim 1 corresponds to a combination of the claims 1 and 2 as filed. However, this is not correct.

59   In the Defendants' view, the subject matter of claim 1 as granted is inadmissibly extended insofar as claim 1 requires that at least one network interface means be coupled between one of the modules and the network. This is disclosed neither in the originally filed dependent claim 2 nor in the description of the patent application. In particular, the delimitation of the network interface means from the network itself cannot be found in the patent application. Furthermore, the original application does not disclose that there is more than one network interface between a module and the network. There is always a one-to-one correspondence between modules and network interfaces. Claim 1 as granted, however, allows for multiple modules connected to one network interface. Finally, patent application does not disclose a Passive Network Interface Port (PNIP) coupled between the addressed module (S) and the network and arranging the first and second information of the first module's message as a single address. This is however possible according to the wording of claim 1 as granted.

60   As regards an inadmissible extension, the Defendants also assert that claim 1 allows for more than one address translation means in one interface means, even in a PNIP. However, throughout the patent application, it is only disclosed that "one" address translation means is present in the respective ANIP.

61   Finally, the Defendants argue that the originally filed application does not disclose that determining the selected location of the addressed module takes place in "the network interface." Neither the original claims nor the original description indicate that this determination is carried out by the network interface. Claims 1 and 2 as filed do not even support that there is a "network interface" in addition to the "network interface means", i.e. two distinct entities. The Defendants also argue that only the ANIP can be the module associated to the first (master) module. However, the patent application does not disclose that the ANIP "determines" "the selected location" of the addressed module based on the single address. This feature cannot be disclosed for the following reason either: the feature requires that something is determined which is already known, namely "the selected location". However, the entire claim 1 does not comprise any "selecting" step to which it can be referred here. If one would argue that the selection has already taken place before the first module provides the first and second information, then there is no determination necessary, since all information is already given by the first module.

62   Furthermore, the Defendants are of the opinion that claim 1 of the patent-in-suit lacks novelty. First, it has to be taken into account that the patent-in-suit does not legitimately claim the priority of European patent application 02079196 filed on 8 October 2002 (Exhibit BP-CR 6). Claim 1 of the priority document does not contain the network interface means according to the claimed technical teaching, nor the translation means, nor the selected location of the addressed module. Moreover, these features are not disclosed in the remainder of the priority document. Consequently, WO 2004/044681 A2 (Exhibit BP-CR 7) is prior art under Art. 54 (3) EPC. Since the technical teaching of claim 1 of the patent-in-suit is disclosed in US 5,349,652

(Exhibit BP-CR 1) as well as in EP 1 091 301 A2 (Exhibit BP-CR 2), Kumar et al., "A Network on Chip Architecture Design Methodology", IEEE, April 2002 (Exhibit BP-CR 3), and WO 2004/044681 A2 (Exhibit BP-CR 7), the claimed technical teaching is not novel.

63 Finally, the Defendants argue that claim 1 of the patent-in-suit is rendered obvious by a combination of any of BP-CR 1, BP-CR 2, or BP-CR 3 with EP 0 717 360 A2 (Exhibit BP-CR 4), a combination of BP-CR 3 with BP-CR 2, or a combination of BP-CR 1 with Dally et al,. "Route Packets, Not Wires: On-Chip Interconnection Networks", DAC 2001 (Exhibit BP-CR 5). The Defendants argue that, if the claimed address translation means is not disclosed in one of the documents BP-CR 1, BP-CR 2, or BP-CR 3, this is suggested to the skilled person by BP-CR 4. If one would assume that a network within the meaning of claim 1 does not include buses and bus systems, BP-CR 5 provides an incentive to prefer such a network over a bus.

64 The <u>Claimant</u> considers the patent-in-suit to be valid. The subject matter of its claim 1 is not inadmissibly extended beyond the content of the patent application. The phrase "associated to" in filed claim 2 has been clarified in granted claim 1 to specify that the network interface is "coupled between" one of the modules and the network. Although the exact wording used is different, the Claimant takes the view that the meaning of the phrase corresponds to the claimed feature. As to the number of network interface means present which are coupled between only one module and the network, nothing has been amended compared to claim 2 as originally filed. Furthermore, the network interface means of claims 1 and 2 as filed are in no way limited to specific active or passive network interface ports (ANIP or PNIP), nor are they in granted claim 1. The Claimant is also of the opinion that the claims 1 and 2 as filed already included embodiments with more than one address translation means in one network interface means. The same is disclosed in the description of the patent application. In this regard, the subject-matter of claim 1 as granted is not inadmissibly extended. Regarding the network interface determining the selected location of the addressed embodiments based on the single address, the Claimant takes the view that there is no distinction between the terms "network interface" and "network interface means" used in the claims. They depict the same entity. Furthermore, this feature of claim 1 as granted is not limited to specific interface means in form of an ANIP. At last, there is no contradiction in determining a selected location as the fact that "the selected location" is "determined" was already present in originally filed claim 1. In any event, if the objection of added matter were seen differently, the Claimant considers that the related deficiencies are eliminated by the auxiliary requests 1 to 4.

65 Finally, the Claimant is of the opinion that the teaching of claim 1 of the patent-in-suit is novel and inventive. Firstly, it should be noted that the priority of the patent-in-suit is correctly claimed. The skilled person can derive the subject matter of the claim directly and unambiguously from the priority application as a whole. Consequently, Exhibit BP-CR 7 is not part of the state of the art. Irrespective of this, Exhibit BP-CR 7 does not disclose the claimed invention, nor do Exhibit BP-CR 1, Exhibit BP-CR 2, and Exhibit BP-CR 3. The interconnect in Exhibit BP-CR 1 and Exhibit BP-CR 2 does not refer to a network on chip. Therefore, network interface means according to the invention are also not the subject of these prior art

documents. In addition, none of the prior art documents disclose address translation means within the meaning of the patent-in-suit. Consequently, the determination of the addressed module or the selected location of that module based on a single address does not take place. In some cases, there are not even messages comprising first and second information within the meaning of claim 1.

66   This is also the reason why the invention under the patent-in-suit is not obvious to the skilled person from any of the combinations of prior art documents as asserted by the Defendants.

Attacked embodiment

67   The Claimant considers the "infringing embodiments II and IV" as the attacked embodiments in general and not limited to specific models. All products which incorporate, implement, utilise, include, or otherwise comprise NoCs designed using tools from the company Arteris Inc. ("Arteris NoC") or NoCs which are materially similar (core-identical) to such Arteris NoCs are attacked. The Claimant argues that it is sufficient to demonstrate that a sample of the attacked embodiment, here: the Snapdragon 8+ Gen. 1, realises all features of the asserted claims. For all other attacked embodiments, it is sufficient to state that they are 'core-identical' or 'materially similar' as the Claimant did. As long as the Defendants do not argue differently, they must be considered as infringing.

68   The Defendants consider only the processor Snapdragon 8+ Gen. 1 as attacked embodiment because the Claimant merely bases its infringement allegation on this single IC model. They argue that the Claimant, instead of identifying only this model and relying on similar models being included, has chosen to explicitly name a large number of models that are also said to be attacked. But then the Claimant must also show that all of these models use the patent-in-suit, because all of these are at issue. Otherwise, Defendants would be burdened with reviewing all of the named products and reply accordingly, which would be inappropriate. The Claimant has however not provided any reasons as to why the other 200+ listed "infringing embodiments II" should be "core-identical" or "materially similar" to that model with regard to the patent-in-suit. Insofar, the Claimant's statements are inconclusive. At least one example, the processor MSM6000 uses fundamentally different technology than the Snapdragon 8+ Gen. 1 as it has no NoC. Beyond the MSM6000, there are further models listed which were already publicly available before the priority date of the patent-in-suit without using any NoC technology.

Infringement

69   The Claimant takes the view that the infringing embodiments II and IV realise the features of claim 1. The Qualcomm NoC ICs are integrated circuits comprising at least two modules, for example a central processing unit, a graphics processing unit and/or a secure processing unit.

70   The Claimant asserts that the infringing embodiment II – the Qualcomm NoC ICs – comprise the Arteris NoC designed according to the Arteris NoC Chapter. This could be inferred from the fact that, according to the press releases and Arteris' statements on its website, the Defendants use Arteris NoC IP technology for over a decade at least in their Snapdragon

application processors, LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products and even acquired Arteris NoC technology including Arteris employees in 2013. In the Claimant's view, this shows that the Defendants rely on Arteris NoC technology in their ICs. Irrespective of this and even if the infringing embodiment II does not implement the Danube NoC IP blocks library and the Qualcomm NoC design tool does not make use of the NTTP packet structure, it can be inferred from the Defendants' submissions that the infringing embodiment II realises the teaching of claim 1 of the patent-in-suit.

71 The Claimant states that messages within the meaning of the patent-in-suit are transferred between the modules as the Arteris NoC transfers requests and responses between the modules according to the Arteris NoC Chapter.

72 The Claimant argues that the requests contain first and second information within the meaning of the patent-in-suit. Using Arteris NoC, the requests are first issued in the third-party protocol of the master module, for example in the AHB protocol. In this regard, the Arteris NoC Chapter refers to 32-bit AHB addresses that are provided to the master or initiator NIU. In order to arrive at their destination, the requests must contain addressing information which tells the NoC where the requests are addressed to. In particular, the Claimant believes that the requests contain information indicative for the location of the addressed slave within the Arteris NoC and the location within the slave, corresponding to the teaching of the patent-in-suit. The Claimant points out that, regardless of this, the Defendants have admitted that the modules in the infringing embodiments ███████████████████████████████████████ ██. According to the Claimant, it is common knowledge that every unique memory location within a system, such as a Network-on-Chip (NoC), has a specific address which identifies both the precise location within a module and the module itself within the larger system. Consequently, the message issued by the first module must include first and second information within the meaning of claim 1.

73 According to the Claimant, the infringing embodiment also comprises network interface means within the meaning of claim 1 as the Arteris NoC makes use of NIUs which connect IP blocks (i.e., modules) to the network. These NIUs manage the communication between the modules and the network by (amongst others) translating third-party protocol transactions into equivalent NTTP packet sequences and vice versa. In accordance with the Arteris NoC Chapter, initiator NIUs connect a master module to the NoC and convert the third-party protocol of the master to the NTTP protocol. In the same way, target NIUs connect a slave module to the NoC and performs protocol translations.

74 The Claimant is of the opinion that the infringing embodiment comprises address translation means within the meaning of the patent-in-suit. According to the Arteris NoC Chapter, the initiator NIU has a Translation Table. This table receives the addressing information as provided by the master module from the NIU including the first and second information and returns the packet header and necker information that is needed to access the NTTP address space, including the Slave address, the Slave offset and the Start/Stop offset. This information forms the single address required by claim 1.

75 The Claimant points out that regardless of the Arteris NoC Chapter, the Defendants have stated that the infringing embodiments make use ████████████████████████████, Therefore, an address translation table is present █████████████████████████████████ ██ ████████████████. According to the Claimant, ████████████████████████████████ ██ ██ ██ ████████████████████████████████ as can be derived from the Defendants' own statements. Accordingly, if no arranging takes place in the infringing embodiments the message could not be forwarded via the network to its intended target. The outcome of this "arranging" is the single address. The Claimant notes, that, as a result, the underlying design and principles which the Defendants allege to use in the infringing embodiments are identical to those described in the Arteris NoC Chapter.

76 The Claimant further argues that the address translation means of the infringing embodiment is adapted to determine which module is addressed based on that single address as the Arteris NoC Chapter explains that the Translation Table returns the packet header and necker information "that is needed to access the NTTP address space". In other words, the single address allows to determine the addressed location in the NTTP address space, which requires knowledge about which slave is addressed. According to the Claimant, the same is valid for the network interface means which are adapted to determine the location of the addressed module. Furthermore, the Arteris NoC Chapter describes that the header and necker cells contain information "relative to routing […] and the packet target address". The necker in the request packet provides "detailed addressing information to the target". This information is thus included in the single address, and thus, based thereupon, the single address allows determining which module is addressed as well as determining the selected location of the addressed module. According to the Claimant, the Arteris NoC Chapter also explains that the target NIU maps the third-party protocol address space from the NTTP address space "using the slave offset, the start/stop offset, and the slave address fields". Therefore, the target NIU is able to determine the addressed slave and the location of the addressed slave based on the single address, so that it contains the required information for the address translation means to do the same.

77 In the Claimant's view, a determination of the addressed module and its location is also performed by the address translation means if the infringing embodiment does not use Arteris technology because the Defendants themselves state that the infringing embodiments comprise ██ ██ ████████████. The logic is to be regarded as the address translation means. It is adapted to determine which module is addressed based on the single address provided as ████████ ██. The logic also determines the selected location of the addressed module. This is core principle ████████████

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██████ as described above. ██
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78 The Defendants are of the opinion that, even if one assumed that the Qualcomm NoC products would be described by the Arteris NoC Chapter, this documentation would not show a realisation of the teaching of claim 1 of the patent-in-suit. They point out that the Claimant refers to the Arteris NoC Chapter and submits that the network interface unit receives a 32-Bit AHB address and returns the packet header and necker that is needed to access the NTTP address space. However, according to the Defendants, the Claimant does not explain which information is included in the AHB address and – if at all – which bits of the AHB address shall equate to a "first information" and a "second information". Notwithstanding this, the document cited by Claimant shows that a single address is provided by the first module such that the allegedly first and second information are already arranged as a single address from the outset. According to the Defendants, the Claimant does not show how the information in the "Slave address" field and the "Slave offset" field of the NTTP packet structure relate to the alleged first and second information, nor how these address fields, which are two distinct portions of a data packet, are used together to determine which module is addressed and furthermore being used together to determine the selected location of the addressed module. Therefore, the documents used as the basis of the infringement argument by the Claimant neither show the message issued by the first module with the first and second information, nor any arranging of first and second information in a single address. Since no single address is used, the Claimant has also failed to show that any single address is used for actual addressing.

79 Irrespective of this, the Defendants even dispute that Qualcomm NoC products, i.e. the infringing embodiments II and IV, were designed identical to "Arteris NoCs" described in Chapter 11 of the book "Networks-on-Chips Theory and Practice", submitted as Exhibit 11. The Defendants contest that the Arteris NoC Chapter describes NoCs on Qualcomm chips. It is rather directed to proprietary Arteris technology which differs from the design used for Qualcomm NoCs. The Defendants are of the opinion that the press releases relating to Arteris NoC technology used in the Defendants' processor applications and to the acquisition of Arteris technology by Qualcomm in 2013 do not support Claimant's allegation that any NoCs in Qualcomm chips are identical to any Arteris NoCs. The Defendants state that this allegation is factually incorrect. According to the Arteris NoC chapter, Arteris proposes a complete commercial solution for SoC communication architecture, which is based on the Danube NoC IP block library. However, the Qualcomm's design tool does not comprise the Danube NoC IP block library.

80 The Defendants state that the Qualcomm NoC products does actually not implement the technical teaching of claim 1 of the patent-in-suit. ██████████████████████████████
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82 The Defendants further state that ███████████████████████████████████████
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███████████████████████████████████. The Defendants explain that a route is a set of
information indicating for each switch in the NoC from which of its ports the packet is to be
sent out. The Defendants point out that, as confirmed by the patent-in-suit, a route is no
address, but an address can be decoded from it in order to obtain the route. ██████████████
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██████. The route does not contain any information which module is addressed and about a location within the addressed module, but only the path information to the network interface connected to the addressed module, since the route only guides the packet up to the network interface of the addressed module. As a consequence, the network interfaces of the Qualcomm NoC products do not provide the claimed single address containing the result of an arranging of two received pieces of information.

83 Finally, the Defendants argue that in the accused embodiments, neither the addressed module nor the location of this module is determined based on a single address. Rather, ████████

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84 Consequently, according to the Defendants, neither independent claim 5, nor the dependent claims 2 to 4 are realised.

Infringing Acts

85 The Claimant argues that Defendants 3) and 4) offer, distribute, import and store the attacked embodiment, inter alia, in Germany and France. Defendant 3) is responsible for the website "www.qualcomm.com" and advertises the attacked embodiment there. Additionally, Defendant 3) provides a "Sales Support" and a list of distributors on its website, where the infringing embodiments can be purchased. These partners are verified to offer, sell and recommend products by Defendant 3) and Defendant 4). Defendant 4) is listed on the footer of the website www.qualcomm.com/ and its subdomains as follows: "Snapdragon and Qualcomm branded products are products of Qualcomm Technologies, inc. and/or its subsidiaries." The Claimant therefore takes the view that Defendant 4) is offering the infringing products on the Website because without the consent no offering would be possible.

86 The Claimant further states that Defendant 4) sells products including the attacked embodiments to manufacturers that use, amongst other products the attacked embodiments, to include them in a broad range of devices, including but not limited to mobile devices,

wireless networks etc. On their website an overview of Defendants' 3) and 4) business partners is provided. The list includes German and French partners, but also international partners, manufacturing mobile devices which are sold in Germany and France. The Defendants 3) and 4) know or even actively support that products in which their infringing embodiments are built in are distributed in Germany and France. In particular, Defendants 3) and 4) distribute their infringing ICs to Samsung Electronics Co., Ltd., the former Defendant 1), for implementation and use in its electronic devices. Furthermore, Defendant 3) and Defendant 4) import and store their ICs – which are also predominantly manufactured in Asia – throughout Europe and especially in Germany and France, in particular for the purpose of distribution.

87   The Claimant further asserts that Defendant 5) markets, sells and distributes products of Defendant 3) and Defendant 4) in Europe, especially in Germany and France. It infers this from Defendant's 5) entry in the German company register. According to the Claimant, it is at least undisputed that Defendant 5) offers the infringing embodiments in France and in Germany. As far as the Defendants dispute that the Defendant 5) has placed the infringing embodiment on the market or imported or stored the same in Germany and/or France during the lifetime of the patent-in-suit, it is sufficient to help someone to place the attacked embodiments on the market. This is exactly what Defendant 5) did.

88   The Defendants state that no Samsung devices containing Qualcomm ICs were/are offered, placed on the market, imported and/or stored in Germany and/or France by the Defendants 3) and 4). Rather Samsung did/does so – and appears now, after the settlement with the Claimant, to be entitled to do so. Moreover, neither Defendant 3) nor Defendant 4) has itself placed on the market, imported and/or stored any Qualcomm NoC products in Germany and/or France during the lifetime of the patent-in-suit. Nor did the Claimant present the requirements of a "wilful collaboration" for the alleged attribution of infringing acts. In the Defendants' view, referring to "collaborators" shown on the website www.qualcomm.com/products/ automotive/partners is not sufficient, taking also into account that there is no relation to the Qualcomm NoC products. The Defendants are of the opinion that the mere position of Defendant 3) as a parent company of the Qualcomm group cannot establish their liability as such, as this would lead to a strict liability of the top level entity. Even if one assumes that Defendants 3) and 4) know that at least some of the Qualcomm NoC products finally found their way on the market in Germany and/or France, this knowledge alone cannot establish a liability of the, themselves non-selling Defendants 3) and 4).

89   Insofar as the Claimant has stated that the Defendants 3) and 4) distribute their ICs to the former Defendant 1) for implementation and use in its electronic devices, the Defendants are of the opinion that these acts of distribution cannot constitute infringing actions in Germany and/or France since the Defendant 1) is located in the Republic of Korea. With regard to the alleged "offering" of the Snapdragon 8+ Gen. 1, the Defendants consider the Claimant's statements to be inconclusive.

90   The Defendants state that the Defendant 5) did not place on the market in Germany and/or France any Snapdragon 8+ Gen. 1, nor did it import and/or store any Snapdragon 8+ Gen. 1 into/in Germany and/or France during the lifetime of the patent-in-suit. Beyond that, the Claimant merely refers to the excerpt from the German company register which does not reflect what Defendant 5) actually does and did over time.

Exhaustion

91   The Defendants further invoke the principles of exhaustion and therefore request that the Claimant and third parties (Samsung, Arteris) be ordered to produce several patent license agreements. The Defendants are of the opinion that the claims asserted by Claimant are unfounded to the extent that products are concerned, which fall under the scope of the license agreements in place between Claimant and RPX Corporation coming into effect as of 31 May 2024 ("RPX Agreement") on the one hand and between RPX and Samsung and RPX and Arteris on the other. The Claimant's rights must be exhausted with regard to the allegedly infringing products (i) manufactured and supplied by Samsung to Qualcomm and/or (ii) using "tools" and/or "NoC technology" from Arteris, if such use should form the basis for assuming infringement of the patent-in-suit). Insofar as Claimant argues that chips manufactured by Samsung and supplied to Qualcomm were excluded from the license, it must be taken into account that exhaustion is a legal effect provided for by law which cannot be circumvented by contractual agreements. Hence, the Claimant itself has shown that any chips supplied by Samsung to Qualcomm are licensed and, insofar, the principle of exhaustion applies. Even if "Arteris was merely granted a covenant to sue last", exhaustion is not excluded as the consent of the patentee to distribute the product does not necessarily have to be in the form of a license.

92   The Defendants further argue that the claims asserted by the Claimant are also inadmissible or at least unfounded, to the extent that the Qualcomm NoC products supplied by the Defendants were used in vehicles of the Volkswagen group. This objection is based on the Covenant not to sue included in the settlement agreement(s) between Claimant and Volkswagen AG and Audi AG and is raised as a defense by Defendants with regard to all Qualcomm NoC products supplied directly or indirectly by any of the Defendants.

93   The Claimant believes that the Defendants cannot successfully rely on an exhaustion defence. The RPX Agreement explicitly excludes the chips manufactured by Samsung and supplied to Qualcomm from the license granted to Samsung (via RPX). Additionally, also Arteris did not get a license from the Claimant.

Statutory limitation of claims

94   The Defendants are further of the opinion that the claims asserted by the Claimant in the Statement of claim are partially time-barred. For each individual claim, they explain why and to what extent they believe it is time-barred under the respective national German or French law. In particular, they argue that Philips must have known already way before 2020 that the attacked embodiment makes use of the patent-in-suit, if following the infringement mapping of Claimant.

95 The <u>Claimant</u> argues that national statute of limitations does not apply to the claims asserted, but rather that Art. 72 UPCA applies, the requirements of which, however, are not met.

<u>Proportionality</u>

96 Finally, the <u>Defendants</u> take the view that the requests must at least be rejected for lack of proportionality, which the <u>Claimant</u> contests.

<u>GROUNDS FOR THE DECISION</u>

97 Both the Counterclaim for revocation and the Infringement action are admissible, but the Counterclaim is successful on the merits, the Infringement action is unfounded.

Part 1: <u>Admissibility</u>

98 The Counterclaim for revocation and the Infringement action are admissible

A   <u>Infringement action</u>

99 The Claimant is entitled to bring the Infringement action before the Unified Patent Court pursuant Art. 47 (1) UPCA, because the Claimant is deemed to be the proprietor of the patent-in-suit.

100 Pursuant to Rule 8.5 (a) RoP, in relation to the proprietor of a European patent, the person entitled to be registered as proprietor under the law of each Contracting Member State in which such European patent has been validated shall be treated as the proprietor whether or not such person is in fact recorded in the register of patents. However, pursuant to Rule 8.5 (c) RoP, there is a rebuttable presumption that the person shown in each national patent register and the European Patent Register is the person entitled to be registered as proprietor.

101 The rebuttable presumption means that the burden of substantiation and proof now lies with the Defendant. He must substantiate that the Claimant is not the proprietor of the patent-in-suit and that the entry in the register is therefore incorrect. It is not sufficient to simply dispute the ownership of the patent or the effectiveness of a patent assignment. Rather, the Defendant must present specific facts from which it can be concluded that the Claimant is not the patent proprietor.

102 In the case at hand, the Claimant is shown as patent proprietor in the concerned national patent registers (see Exhibit P 4 and P 5) and in the European Patent Register (see Exhibit P 3) and is therefore to be considered the patent proprietor. The Defendants have not successfully rebutted this presumption.

103 Insofar as the Defendants object to the Claimant's allegedly late submission of documents such as the PPA and the PA (Exhibit P 24 and P 25), this objection is invalid because it is up to the Defendants to present facts that refute the Claimant's ownership of the patent in suit. However, the Defendants' further submissions are limited to merely disputing the content of the agreements, the fulfilment of the contractual conditions for the patent assignment and the signatories' authority to sign the agreements.

104 The only facts pointed out by the Defendants are the different colours and formats of individual pages of the agreements, which suggest that the agreements were composed of different documents or that only signature pages with different formats were exchanged. However, this and the legal opinions expressed by the Defendants on the interpretation of the agreements and the scope of authority of individual signatories do not allow the compelling conclusion that the entire patent assignment is invalid.

105 As the Claimant is considered the patent proprietor, it is in any case entitled to bring the Infringement action. Whether it is also entitled to claims arising from the patent for the period prior to acquisition of the patent-in-suit is, at most, a question of the merits of the action, unless it is already entitled to assert all claims arising from the patent on the basis of his ownership. However, a decision on this point is not necessary here.

B   Counterclaim for revocation

106 A decision on the Counterclaim for revocation is not precluded by the fact that the Defendants stated in the oral hearing that they saw sense in treating the Counterclaim as a true Counterclaim in case only there was infringement. During the oral hearing, the court merely raised the possibility of a conditional counterclaim for discussion and made it clear that such a conditional counterclaim could be reflected in a corresponding request. However, the possibility of a conditional Counterclaim was not discussed further by the parties, no case law was cited if any was known at that time (see Local Division Mannheim, decision of 5 December 2025, UPC_CFI_414/2024), and no formal request was made ("we would see sense …"), in particular, no specific condition was mentioned under which a decision should be made on the counterclaim or not and how the auxiliary requests should be dealt with. In this regard, the Defendants' statement at the end of the oral hearing that they want to set the condition is not sufficient.

Part 2: On the merits

107 The Counterclaim is successful on the merits. The Infringement action is unfounded

A Subject matter of the patent-in-suit

108 The invention of the patent-in-suit relates to an integrated circuit having a plurality of processing modules and a network arranged for transferring messages between processing modules and a method for exchanging messages in such an integrated circuit (Para. [0001]; further on, quotations from paragraphs without reference are those of the patent-in-suit).

I. State of the art, problem and solution

109 With regard to the background of the invention and the state of the art, the patent-in-suit states that systems on silicon show a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions. This is enabled by the increasing density with which components can be integrated on an integrated circuit. At the same time the clock speed at which circuits are operated tends to increase, too. The higher clock speed in combination with the increased density of components has reduced the area which can operate synchronously within the same clock domain. This has created the need for a modular approach. According to such an approach, the processing system comprises a plurality of relatively independent, complex modules. In conventional processing systems the systems modules usually communicate to each other via a bus. As the number of modules increases, however, this way of communication is no longer practical for the following reasons. On the one hand, the large number of modules forms a too high bus load. On the other hand, the bus forms a communication bottleneck as it enables only one device to send data to the bus. A communication network forms an effective way to overcome these disadvantages (Para. [0002]).

110 Networks on chip (NoC) have received considerable attention recently as a solution to the interconnect problem in highly complex chips. The reason is twofold. First, NoCs help resolve the electrical problems in new deep-submicron technologies, as they structure and manage global wires. At the same time, they share wires, lowering their number and increasing their utilization. NoCs can also be energy efficient and reliable and are scalable compared to buses. Second, NoCs also decouple computation from communication, which is essential in managing the design of billion-transistor chips. NoCs achieve this decoupling because they are traditionally designed using protocol stacks, which provide well-defined interfaces separating communication service usage from service implementation (para. [0003]).

111 The patent-in-suit names the articles "A Generic Architecture for On-Chip Packet-Switched Interconnections" by P Guersier (2000), and "A Network on Chip Architecture and Design Methodology" by S Kumar (2002) as technical literature on network on chip technology, known in the state of the art (para. [0004]).

112 Using networks for on-chip communication when designing systems on chip (SoC), however, raises a number of new issues that must be taken into account. This is because, in contrast to existing on-chip interconnects (e.g., buses, switches, or point-to-point wires), where the communicating modules are directly connected, in a NoC the modules communicate remotely

via network nodes. As a result, interconnect arbitration changes from centralized to distributed, and issues like out-of order transactions, higher latencies, and end-to-end flow control must be handled either by the intellectual property block (IP) or by the network (para. [0005]).

113 Most of these topics have already been the subject of research in the field of local and wide area networks (computer networks) and as an interconnect for parallel machine interconnect networks. In this regard, the patent-in-suit refers to the disclosure of EP 1 083 768 A which teaches a method for data transmission in a communication system using IP, a gateway buffer and other specialised devices. Both are very much related to on-chip networks, and many of the results in those fields are also applicable on chip. However, NoC's premises are different from off-chip networks, and, therefore, most of the network design choices must be reevaluated. On-chip networks have different properties (e.g., tighter link synchronization) and constraints (e.g., higher memory cost) leading to different design choices, which ultimately affect the network services (para. [0006]).

114 In the further course of its introduction into the state of the art, the patent-in-suit compares several functions and features of on-chip networks with those of off-chip networks (para. [0007])-[0010]).

115 Among other things, the patent-in-suit points out that introducing networks as on-chip interconnects radically changes communication when compared to direct interconnects, such as buses or switches. This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes. This is in contrast with the prevalent existing interconnects (i.e., buses) where modules are directly connected. The implications of this change reside in the arbitration (which must change from centralized to distributed), and in the communication properties (e.g., ordering, or flow control) (para. [0011]).

116 Traditionally, on a bus all transactions are ordered (cf. Peripheral VCI, AMBA, or CoreConnect PLB and OPB). This is possible at a low cost, because the interconnect, being a direct link between the communicating parties, does not reorder data. However, on a split bus, a total ordering of transactions on a single master may still cause performance penalties, when slaves respond at different speeds. To solve this problem, recent extensions to bus protocols allow transactions to be performed on connections. Ordering of transactions within a connection is still preserved, but between connections there are no ordering constraints (e.g., OCP, or Basic VCI). A few of the bus protocols allow out-of-order responses per connection in their advanced modes (e.g., Advanced VCI), but both requests and responses arrive at the destination in the same order as they were sent (para. [0012]).

117 In a NoC, ordering becomes weaker. Global ordering can only be provided at a very high cost due to the conflict between the distributed nature of the networks, and the requirement of a centralized arbitration necessary for global ordering. Even local ordering, between a source-destination pair, may be costly. Data may arrive out of order if it is transported over multiple routes. In such cases, to still achieve an in-order delivery, data must be labeled with sequence

numbers and reordered at the destination before being delivered. The communication network comprises a plurality of partly connected nodes. Messages from a module are redirected by the nodes to one or more other nodes. To that end, the message comprises first information indicative for the location of the addressed module(s) within the network. The message may further include second information indicative for a particular location within the module, such as a memory, or a register address. The second information may invoke a particular response of the addressed module (para. [0013]).

118 For a bus, the command, address, and data are broadcasted on the interconnect. They arrive at every destination, of which one activates based on the broadcasted address, and executes the requested command. This is possible because all modules are directly connected to the same bus. In a NoC, it is not feasible to broadcast information to all destinations, because it must be copied to all routers and network interfaces. This floods the network with data (para. [0014]).

119 Against this background, the patent-in-suit indicates as an object of the invention to provide an integrated circuit and a method for exchanging messages in an integrated circuit without introducing too many data into the network (para. [0015]).

120 In order to solve this problem, the patent-in-suit provides, among other things, an integrated circuit with the features of claim 1, which can be structured as follows:

1. Integrated circuit comprising

   1.1 a plurality of modules (M, S),

   1.2 a network (N),

   1.3 at least one network interface means (ANIP, PNIP),

   1.4 at least one address translation means (AT).

2. The network (N)

   2.1 is arranged for transferring messages between said modules (M, S),

   2.2 wherein a message issued by a first module (M) comprises (claim feature 1.2)

      2.2.1 first information indicative for a location of an addressed module within the network, and

      2.2.2 second information indicative for a location within the addressed module (S).

3. The at least one network interface means (ANIP, PNIP) (claim feature 1.3)

   3.1 is coupled between one of the modules (M, S) and the network (N)

   3.2 for managing the communication between said associated module (M, S) and the network (N).

4. The at least one address translation means (AT)

    4.1 is arranged in one of said interface means (ANIP, PNIP)

    4.2 for arranging the first and the second information as a single address.

5. Said address translation means (AT) is adapted to determine which module is addressed based on said single address.

6. The network interface determines the selected location of the addressed module (S) based on said single address.

II.   Claim construction

121 An integrated circuit according to the invention shall comprise a plurality of modules, a network, at least one network interface means and at least one address translation means which perform various functions in order to solve the technical problem raised in the patent-in-suit. These terms and their functions as the claim in its entirety require interpretation.

1.   Legal principles

122 In accordance with Art. 69 EPC and the Protocol on its interpretation, a patent claim is not only the starting point, but the decisive basis for determining the scope of protection of a European patent. The interpretation of a patent claim does not depend solely on the strict, literal meaning of the wording used. Rather, the description and the drawings must always be used as explanatory aids for the interpretation of the patent claim and not only to resolve any ambiguities in the patent claim. However, this does not mean that the patent claim merely serves as a guideline and that its subject-matter also extends to what, after examination of the description and drawings, appears to be the subject-matter for which the patent proprietor seeks protection (Court of Appeal, UPC_CoA_335/2023, Order 23 February 2023; Court of Appeal, UPC_CoA_1/2024, Order 13 May 2024; Central Division Munich, UPC_CFI_1/2023, Decision 16 July 2024; Local Division Paris, UPC_CFI_230/2023, Decision 4 July 2024; Local Division Munich, UPC_CFI_233/2023, Decision 31 July 2024; Local Division Hamburg, UPC_CFI_54/2023, 26 August 2024; Local Division Düsseldorf UPC_CFI_363/2023, Decision 10 October 2024; Local Division Düsseldorf UPC_CFI_373/2024, Decision 31 October 2024).

123 The patent claim is to be interpreted from the point of view of a person skilled in the art. When interpreting a patent claim, the person skilled in the art does not apply a philological understanding but determines the technical meaning of the terms used with the aid of the description and the drawings. A feature in a patent claim is always to be interpreted considering the claim as a whole (Court of Appeal, UPC_CoA_1/2024, Order 13 May 2024). From the function of the individual features in the context of the patent claim as a whole, it must be deduced which technical function these features actually have individually and as a whole. The description and the drawings may show that the patent specification defines terms independently and, in this respect, may represent a patent´s own lexicon. Even if terms used in the patent deviate from general usage, it may therefore be that ultimately the meaning of the terms resulting from the patent specification is authoritative (Central Division Munich,

UPC_CFI_1/2023, Decision 16 July 2024; Local Division Düsseldorf UPC_CFI_373/2024, Decision 31 October 2024).

2. <u>Person skilled in the art</u>

124 The skilled person is to be defined as an electrical engineer or computer scientist with practical experience in the field of SoC and NoC technologies and with general notions of computer networks and with basic knowledge of electrical engineering or computer engineering acquired as part of his/her studies. This definition partly corresponds to the definition suggested by the Claimant. However, insofar as Claimant argues that the skilled person would not be a specialist in, for example, computer networks, this is not convincing. As shown by the background section of the patent-in-suit, computer network technology cannot be considered a remote field from NoCs and is therefore generally known to the skilled person.

3. <u>Modules</u>

125 According to the description of the patent-in-suit, an integrated circuit has a number of features and functions which are performed by modules due to an increase in complexity and clock speed and, as a result, a preferred modular approach (cf. para. [0002]). Modules within the meaning of claim 1 of the patent in suit can therefore be understood as functional subunits consisting of one or more electronic components and performing specific tasks within an integrated circuit. According to features 2.1 and 2.2, modules communicate with each other by sending and receiving messages which are transferred over the network between the modules. In this respect, claim 1 distinguishes the modules from the network and also from the network interface means and the address translation means. Examples of modules are central processor units and memories, and with regard to the type of communication, a distinction can be made between a master module and slave modules (cf. para. [0031]).

4. <u>Network</u>

126 The integrated circuit according to the invention further comprises a network. Pursuant to feature 2, the network is arranged for transferring messages between the modules. However, not every arrangement that is suitable for transmitting messages between several modules can be regarded as a network within the meaning of claim 1. Taking into account the description and the drawings of the patent-in-suit, a network according to claim 1 must instead be understood as a network on chip (NoC) which connects the several modules of the integrated circuit by means of lines connected via nodes, so that the lines can be shared, which structures and manages these lines, and which decouples communication from the actual computing tasks of the modules by using a separate protocol stack, which provide well-defined interfaces separating communication service usage from service implementation.

127 If the description of the patent-in-suit refers to a network, then it always refers to a network on chip as defined above (para. [0003]). The patent-in-suit delimits the network on chip from other

existing on-chip interconnects like buses, switches, or point-to-point wires (para. [0005] and [0011] to [0014]) as well as from local and wide area networks (computer networks or off-chip networks) (para. [0006] to [0010]).

128 In particular, an interconnect established solely via buses or other point-to-point connections cannot be regarded as a network within the meaning of the patent-in-suit and claim 1. This does not preclude the use of a bus within a network on chip. However, the patent-in-suit expressly states that a network (on chip) differs from existing on-chip interconnects such as buses, switches, or point-to-point wires, where the communicating modules are directly connected to each other. In contrast, the modules in a network on chip communicate remotely via network nodes, which raises other issues, for example interconnect arbitration changes from centralised to distributed and out-of order transactions, higher latencies, and end-to-end flow control must be handled (para. [0005] and [0011]). Therefore, a network within the meaning of claim 1 cannot be established exclusively by a bus system, point-to-point connections or other direct connections between the modules.

129 The description of the patent-in-suit deals with the problem of transaction ordering in more detail (para [0012] and [0013]). However, the specific technical problem arises from the destination name and routing in a network on chip as defined above and makes it clear that buses and bus systems as such cannot be regarded as a network within the meaning of the patent-in-suit. The patent description states that for a bus, all modules are directly connected to the same bus. The command, address, and data broadcasted on this interconnect therefore arrive at every destination, of which one activates based on the broadcasted address, and executes the requested command. In a network on chip, it is not feasible to broadcast information to all destinations, because it would have to be copied to all routers and network interfaces and thereby flooding the network with data (para. [0014]). This is where the object of the invention addressed by the patent-in-suit comes in as this is to provide an integrated circuit and a method for exchanging messages in an integrated circuit without introducing too much data into the network (para. [0015]). However, this presupposes that a network on chip as defined above is used in the integrated circuit and not a bus or other point-to-point connection.

130 Most of the typical features of a network on chip are also reflected in claim 1. In particular feature groups 3 and 4 reflect the decoupling of computation from communication (cf. para. [0005]) because the network interface means is coupled between one of the modules and the network and manages the communication between them (feature group 3). Claim 1 also presupposes that the network uses protocol stacks (cf. para. [0005]) that are in principle unknown to the modules. This requires network interface means (cf. para. [0005] and feature group 3) and address translation for the purpose of transferring messages over the network using the specific network protocol. According to claim 1, address translation is performed by the address translation means (features 4-6). Regularly, buses and modules connected by a bus need neither specific interface means nor address translation means as specified by claim 1 of the patent-in-suit even if a bus system does not exclude those means.

131 Another interpretation of claim 1 cannot be based on the first embodiment of the patent description and the explanation that the interconnect is embodied as a network on chip NoC which may include wires, bus, time-division multiplexing, switch, and/or routers within a network (para. [0029]). As already mentioned, the term "network on chip" or "network" within the meaning of claim 1 does not exclude buses within the network. However, a single bus or a pure bus system cannot be understood as a network in the sense of the patent-in-suit. Nor can this be inferred from the passage quoted above as it states "bus (…) within a network". Insofar as the patent-in-suit expressly states that this scheme (addressing performed by the address translation means within the network interfaces) is backward compatible with buses (para. [0018]), this does not imply that its NoC may be composed solely of buses, but rather that it is also designed to replace or interoperate with earlier bus-based architectures.

5. Network interface means

132 As required by claim 1 and already explained above, the at least one network interface means is coupled between one of the modules and the network and serves to manage communication between the module and the network (feature group 3). As can be inferred from the term "interface" and from feature group 3, which describes the network interface means coupled between the modules and the network and managing the communication between the modules and the network, the network interface is a unit distinguishable from both the module and the network, which is located at the boundary between the module and the network and performs functions independently of these units.

133 Beyond the term "interface" which distinguishes the network interface means as a functional unit from the module and the network, the term "coupled between" establishes a structural feature and requires at least a physical separation between the network interface means on one side and the module and the network on the other. The expression "coupled between one of the modules (M, S) and the network" implies that the network interface is connected between the module and the network without being part of either of the two other units. It indicates a structural distinction implying a physical separation between these components.

134 The patent-in-suit describes the function of the network interface means (see feature 3.2) in connection with a preferred embodiment in such a way that it manages the communication of the respective modules and the network, so that the modules can perform their dedicated operation without having to deal with the communication with the network or other modules. In particular, the network interface means can send read and write requests and operations between each other over the network (para. [0030]). Furthermore, at least one of the network interface means incorporates at least one address translation means in accordance with feature 4.1 and thus serves to translate addresses (see Para. [0024], [0034] and [0039]) or at least to arrange information as a single address (feature 4.2). This is necessary to ensure that the network can transfer the messages to the addressed module at all. The network interface means is an independent functional unit in the sense that it frees the module from address mapping to the addressed modules and also allows the network to be used more efficiently

because the network interface takes over the addressing (para. [0018]). This presupposes a spatial-physical separation of the network interface means from the network and the module, ensuring that the latter are relieved of address translation and other interface functions, which are performed independently by the network interface means.

135 Against this background, it is not sufficient for the Claimant to emphasise in the oral hearing the term "interface" as a face between a network and a client and its function as means of managing the transportation of data and instructions between the client and the network. It is not just a question of the location of the network interface means on a chip, regardless of whether it is even in the module as a functional unit. Rather, it can be inferred from the additional wording "coupled between" and from the intended separation of computation and communication which is achieved by coupling the network interface means between the module and the network that a physical separation of the network interface means on the one hand and the module and the network on the other is required. Insofar as the Claimant referred in the oral hearing to the article "A Network on Chip Architecture and Design Methodology" of Kumar et al. (Exhibit BP CR 3) and its figure 1 in order to explain that the skilled person does not imply a specific location or spatial arrangement of a network interface on a chip, this cannot be accepted. Exhibit BP CR 3 is not material for the claim construction. Even if it is mentioned in the patent-in-suit, the details regarding the location of the network interface means are not relevant in this context, neither in Kumar itself nor in the description of the patent-in-suit with regard to Kumar. The mere mention of the Kumar article as existing technical literature in the background section does not serve to incorporate its specific disclosures; for the skilled person, it is a general bibliographic pointer, not a source for interpreting the distinct teaching of the invention.

136 As a result, the network interface means are to be considered as independent units that can be physically distinguished from the modules and the network by their location at the boundary between the network and the modules and by their function of managing communication between the modules and the network. Nothing else can be inferred from the drawings of the patent-in-suit. These are schematic representations that do not show any details of the spatial-physical relationship between network interface means on the one hand and modules and the network on the other. Rather, they only illustrate the functional relationship between the network interface means, the modules and the network.

137 It should be noted that there is no difference between the term "network interface means" used in feature 3 of claim 1, the term "interface means" used in feature 4.1 of claim 1 and paragraph [0019] and [0020], and the term "network interface" used in feature 6 of claim 1 and in paragraph [0030] ff. As can be seen from the wording of claim 1 itself and the passages cited, the skilled person directly and unambiguously understands that the patent-in-suit uses the terms synonymously.

6. Message comprising first and second information

138 In the context of the interpretation of the term "network interface means", the address translation means and the function of address translation have already been mentioned. To better understand this, feature group 2.2 and the messages to be transferred need to be explained in more detail.

139 According to feature group 2.2, a message issued by a first module comprises first information indicative for a location of an addressed module within the network and second information indicative for a location within the addressed module. The wording of claim 1 is silent on the structure and the specific content of the message. Although the message comprises first and second information, feature group 2.2 leaves open how this information is specified within the message and how it is structured. The term "indicative" clarifies that the message does not have to directly indicate the location of the addressed module or the location within the addressed module. It does not even seem to be necessary for the message to comprise two different pieces of information in the sense of two different parts of the message. Rather, information within the meaning of feature group 2.2 can also be understood as an abstract concept. Information is what can be derived from the message through calculation, translation, interpretation or other means of decoding. Accordingly, it is sufficient if first and second information can be obtained from the message issued by the module. Claim 1 does not impose any requirement as to whether the information is explicitly contained in the message, whether the first and the second information can be derived from different parts of the message, or whether one and the same part of the message makes it possible to simultaneously deduce information about the location of the addressed module and about the location within the addressed module.

140 This interpretation of claim 1 and its feature group 2 does not contradict the wording of the claim. It is supported by the interaction with other claim features and, based on this, by the mode of operation of the integrated circuit according to the invention.

141 Feature group 4 provides for at least one address translation means which has already been mentioned before in the context of the network interface means. The term "address translation means" itself makes it clear that the function of this means is to translate addresses. In particular, the address translation means must be capable of arranging the first and second information in a single address. This implicitly requires that this information has been previously derived from the message sent by the module associated with the corresponding network interface means. It is the address translation means arranged in this network interface means which, as the term "translation" suggests, has the task of ascertaining the first and second information. The claim leaves open how the address translation means accomplish this. The term „translation" suggests that some kind of computing or mapping is not precluded. But then it is also acceptable for the first and second information to be contained in the message only in abstract form, as long as the address translation means can derive this information from the message in order to arrange it into a single address. Pursuant to features 5 and 6, this single address is then the basis for determining the addressed module and the

location of the addressed module in order to transfer the message over the network to the addressed module.

142 The description of the patent-in-suit supports this interpretation of claim 1 and feature group 2.2. According to the second embodiment of the patent-in-suit, "a process on a master M may see an address map of 0-FF, which is allocated in the memories of the two slaves S1, S2, i.e. 0 – 7F in the memory of the first slave S1 and 80-FF in the memory of the second slave S2. An address can be decoded at the source to find a route to the destination module" (para. [0031]). The patent description explicitly states that a "connection can be implemented by decoding each transaction address at the active network interface ports ANIP. According to the decoding, the target slave of the transaction is identified" (para. [0033]). In the third embodiment, the decoding of a similar address range (0000-FFFF instead of 00-FF) is performed by an address translation manager AT using an address mapping table (paras. [0034]-[0035]). All this indicates that the master module M does not know the location of slaves S1 and S2 within the network, nor the locations within their memories, but only a global memory address map from 0-FF. However, when the master M selects a memory location from this global address map, it is possible to deduce the slave that hosts the memory with this memory location and the specific location within the memory of this slave. For example, global memory location 0 could represent the first slave S1 and the first memory location within its memory, while memory location 80 could represent the second slave S2 and the first memory location within the memory of this second slave S2. Then a transaction address can be determined comprising a destination identifier and an internal address at the destination (cf. para. [0031]).

143 Even though in the embodiments of the patent description the value of the first bit corresponds to the respective addressed slave, it is important to note that this is only an example and the module sends a message that does not necessarily contain two data sections explicitly representing the first and second information, but rather one global address in the form of a global memory location from which the first information indicating the addressed module and the second information indicating the memory location within this module can be derived by address mapping.

144 The foregoing explanations also clarify how the phrase 'within the network' in feature 2.2.1 is to be understood. Insofar as the feature states that the first information is indicative for "a location of an addressed module within the network", this does not mean that the module is now part of the network. This is already contradicted by the fact that claim 1 clearly differentiates between the network on the one hand and the modules on the other. Instead, the phrase 'location (…) within the network' is to be interpreted as referring to the location of the interface connection through which the module is linked to the network. In the broadest sense, the expression must be understood as identifying the network address associated with that module connection as conveyed by the first information. This is also exemplified in the patent description which states that the global address "is constituted by a network address and a local address. The network address may be the port identifier of the receiving module,

i.e. the port_ID of the passive network interface ports PNIP" (para. [0036]; see also para. [0037]: "The network interface port NIP address (…) are still needed.").

7. Address translation means

145 The preceding explanations lead to the requirements for the address translation means and its function.

146 The address translation means can be regarded as a subunit of the network interface means as it must be arranged in one of said interface means in accordance with feature 4.1 of claim 1. Its function, according to feature 4.2, is to arrange the first and the second information as a single address and, according to feature 5, to determine which module is addressed based on said single address. The claim leaves open whether it also determines the selected location of the addressed module based on said single address as feature 6 refers only to the network interface.

147 Arranging the first and the second information as a single address in feature 4.2 means that the address translation means forms a single address containing the first and the second information in its decoded form so that the module and the location of the addressed module can be determined on the basis of this address. This follows from the term "address translation means", the term "arranging" and the interplay with the other features of claim 1.

148 As already demonstrated, the message issued by a first module may comprise the first and the second information in encoded form and it is the function of the address translation means, as its name already suggests, to derive the first and the second information from the message by translating, computing, mapping or other means of decoding. It can be left open whether the decoding is considered an (unwritten) independent step prior to the arranging step of feature 4.2 or part of the arranging step when interpreted in the light of paragraph [0024], [0034] and [0039]. In any case, it can be inferred from the term "arranging" that the at least one address translation means must be capable of forming an address that can, and generally does, differ from the original message issued by the module and contains the first and the second information. In this respect, the requirement for a single address does not preclude the address having two parts, each representing one piece of information. Instead, the first information and the second information must not be divided in such a way that the first information is located in the address, and the second piece of information is encoded in the associated message or otherwise communicated.

149 Feature 4.2 is the consequence of decoupling the computation performed by the modules from the communication performed by the network interface means (cf. para. [0003]). The patent-in-suit expressly states in the general part of its description that "the addressing is performed by the address translation means" (para. [0018]). This requires the decoding of the first and the second information from the message issued by the module and the arrangement of this information in a (new) single address. Apart from that, claim 1 does not contain any

instructions on how arranging the two pieces of information in a single address can be performed. This can also be done using a mapping table.

150 The further step of determining which module is addressed according to feature 5 must be distinguished from the arrangement step in feature 4.2. According to the technical teaching of claim 1, the address translation means must be capable of performing two steps: first, arranging the first and the second information as a single address, and second, determining which module is addressed based on said single address. This is clear from the two different features, which require different actions by the address translation means, and from the fact, that the second step – determining which module is addressed – is based on the single address. That means that the determination step necessarily presupposes that the single address has been arranged beforehand.

8. Determining which module is addressed and determining of the selected location

151 As already mentioned, the determination step of feature 5 has to be distinguished from the arrangement step of feature 4.2. Finally, claim 1 also requires in feature 6 that the selected location of the addressed module is determined based on the single address.

152 This second determination step needs not necessarily be performed by the address translation means. In this respect, feature 6 differs from feature 6 and merely requires that the network interface performs the second step of determination. The patent description does not contain any information about which unit performs this step of determination. In any case, this second step must be distinguished from the arrangement step of feature 4.2 for the same reasons as the first determination step (see above).

153 Even if it is possible to carry out the determination in accordance with features 5 and 6 together in one single operation, it is essential that two different pieces of information are determined, namely the addressed module on the one hand ("which") and the selected location of the addressed module on the other ("where"). The wording makes it clear that these are not the first and the second information mentioned in feature group 2.2 and in feature 4.2. In particular, determining which module is addressed does not mean that the location of the addressed module within the network is determined, and determining the selected location of the addressed module does not correspond to the location within the addressed module. This would not make sense as the first and second pieces of information have just been derived from the message and arranged in the single address according to feature group 4, and there is no reason why they should now be determined again by the address translation means. Rather, the features 5 and 6 refer to the example already explained in paragraph [0031] and [0035], according to which the global address from 00-FF makes it possible to determine the addressed module (slave S1 if global address from 00-7F or slave S2 if global address from 80-FF) and, consequently, the location of the addressed module, i.e. the network address or port identifier of the network interface port through which the addressed module is accessible.

154 After determining the addressed module and its location, the network interface means can transfer the message via the network to the addressed module at the location determined in accordance with feature 6. It is not part of the technical teaching of claim 1 how the location within the addressed module is determined and how the message is transferred there.

155 During the oral hearing, the Claimant argued for the first time that feature 6 did not constitute a separate determination step, but should be read as a conclusion: because the modules are not intended to deal with the specific addressing of other modules, the address translation means arrange the first and second pieces of information into a single address (feature group 4) and determine which module is addressed on the basis of this single address (feature 5). Because feature 6 is in past tense and the module has already been addressed, this also applies to the selected location of the addressed module. This view is not convincing. It contradicts the clear wording of claim 1 of the patent-in-suit and its feature 6. The technical teaching of claim 1 distinguishes between the determining which module is addressed based on the single address and the determining the selected location of the addressed module based on said single address. The term "addressed module" only serves to differentiate this module from the first module (see feature 2.2 and 2.2.1). It cannot be inferred from this term that the location of this module has already been determined. On the contrary, feature 6 establishes a separate determination step, as also contained in independent claim 5. There are no indications as to why the integrated circuit should behave differently than described in method claim 5. Without specific reasons, it cannot be assumed that a feature such as feature 6 has no significance for the teaching of a patent claim. However, it is precisely this significance that the Claimant attempts to negate through its interpretation, without providing any reason for doing so.

B   Counterclaim for revocation

156 The Counterclaim for revocation is successful on the merits.

I.   Inadmissible extension of the subject-matter of claim 1 as filed

157 The patent is inadmissibly extended, Art. 138 (1) (c), 123 (2) EPC and is to be revoked in its entirety, Art. 65 (2) UPCA.

1.   Legal principles re. "added matter"

158 In accordance with Art. 138 (1) (c) EPC, a European patent may be revoked if its subject-matter extends beyond the content of the application as filed or, if the patent was granted on a divisional application or on a new application filed under Art. 61 EPC, beyond the content of the earlier application as filed (added matter).

159 In order to ascertain whether there is added matter, the Court must ascertain what the skilled person would derive directly and unambiguously using his/her common general knowledge

and seen objectively and relative to the date of filing, from the whole of the application as filed, whereby implicitly disclosed subject-matter, i.e. matter that is a clear and unambiguous consequence of what is explicitly mentioned, shall also be considered as part of its content (Court of Appeal, UPC_CoA_764/2024, UPC_CoA_774/2024, 2 October 2025 – expert e-Commerce/Seoul Viosys; UPC_CoA_382/2024, 14 February 2025 – Abbott/Sibio).

160 Where the patent results from a divisional application, this requirement applies to each earlier application. The subject matter of the granted claim thus may not extend beyond (1) the disclosure of the application as filed for the patent in suit and (2) the disclosure of the original PCT application that entered the regional phase and is the parent application for the divisional application   (Court of Appeal, UPC_CoA_764/2024, UPC_CoA_774/2024, 2 October 2025 – expert e-Commerce/Seoul Viosys).

2.   Present case

161 The subject matter of claim 1 of the patent-in-suit and, consequently, also claim 5 extends beyond the content of the patent application which is the international patent application no. PCT/IB2003/003036, submitted as Exhibit BP_CR 8 (hereinafter: patent application). Claim 1 as granted is derived from claim 1 and 2 disclosed in the patent application, however its subject matter is inadmissibly extended.

a)   Network interface means coupled between one of the modules and the network

162 Feature group 3 cannot directly and unambiguously be derived from the patent application.

163 The subject matter of claim 1 as granted is inadmissibly extended with regard to the arrangement of the "network interface means coupled between one of the modules (M, S) and the network (N)" (claim feature 3.1). As already explained above, this expression requires a structural distinction between the network interface means on the one hand and the modules and the network on the other, which implies a physical separation of these components.

164 The patent application does not contain any literal basis for this structural definition. There are several passages, which deal with the relationship of the network interface means, the module and the network. But none of them literally indicate that the network interface means (or network interfaces) are coupled between the modules and the network, understood as being physically distinguishable between the modules and the network. Nor is this implicitly disclosed in the patent application.

165 Claim 2 originally filed requires that the at least one interface means is "associated to one of the modules." This expression does not exclude the possibility that the network interface means is an integral part of the respective module. Even though the "interface means" differs functionally from the module that provides computation services and the network that provides data transmission services, and even though an interface is typically located on the boundary

between two or more separate components of a computer system, here: the module and the network, across which information can be exchanged between these components, this does not preclude interface means from being part of a module or even a module which also performs interface functions. All of this is covered by the expression "one interface means associated to one of the modules", which is even silent on the relationship between the interface means and the network.

166 Nothing else can be inferred from the description of the patent application.

167 The wording on Page 5, lines 2–7 of the patent application corresponds to claim 2 as filed, as well as the passage on page 7 line 1-3 of the patent application.

168 Furthermore, the description discloses first and second embodiments which comprise network interfaces NI "used as interfaces between the master and slave modules M, S1, S2 and the network" (p. 6 l. 22-29 of the patent application) or "network interfaces ANIP, PNIP between the modules and the router network RN" (p. 6 l. 30-35 of the patent application). The third preferred embodiment disclosed in figure 3 is based on the system according to the second embodiment (see p. 8 l. 4-5 of the patent application) and, therefore, also comprises network interfaces between the modules and the networks. The function of the network interface means is to manage the communication between the module and the network as required by claim 2 as filed and repeatedly described in the patent application (p. 5 l. 1-4, p. 6 l. 25-28; p. 13 l. 28-29 of the patent application; see also p. 6 l. 32-34). Even if these passages mention network interfaces between the modules and the network, they do not directly and unambiguously refer to the physical relationship of the components as it is expressed in the term "coupled between". Rather, the function of the network interface means is mentioned (cf. "network interfaces NI are used as interfaces between (…)", p. 6 l. 22-29 of the patent application). At the very least, no structural definition of where the interface means are located and arranged can be directly and unambiguously derived from these passages.

169 The same applies to the drawings in the patent application, which correspond to those in the patent-at-issue. As already explained, these are schematic representations that do not allow any direct and unambiguous conclusions to be drawn about the spatial-physical arrangement of the components. Even if the network interfaces NI, ANIP and PNIP were to be spatially and physically separated from the modules, this cannot be said in relation to the network. According to the drawings, the network interfaces may also be part of the network.

170 As a result, the patent application teaches that the network interface means are functionally interposed between the modules and the network, managing or controlling communication between them, but the skilled person cannot infer directly and unambiguously that network interface means are coupled between the modules and the network, being structurally interposed between them.

b) The network interface determines the selected location of the addressed module

171 With regard to feature 6, subject matter of claim 1 of the patent-in-suit inadmissibly extends beyond the originally filed patent application. The latter does not disclose that the network interface determines the selected location of the addressed module.

172 The patent application does not specify which unit determines the selected location of the addressed module based on the single address.

173 Claim 1 as filed only requires that "the selected location of the addressed module (S) is determined based on said single address." There is no passage in the patent application that literally recites that "the network interface determines the selected location of the addressed module based on the single address." Instead, the wording of claim 1 as filed is repeated several times in the description of the patent application (p. 4 l. 27-29 and p. 5 l. 21-23 of the patent application). Claim 1 as filed and the passages cited refer to the address translation means as the unit that performs the determination of the addressed module. However, the network interface is neither identical to the address translation means nor is it disclosed in the patent application for determining the selected location of the addressed module.

174 Insofar as the patent application refers to the first information indicative for the location of the addressed module within the network and the second information indicative for the location within the addressed module (p. 4 l. 3-7 and l. 23-25 of the patent application), this explains what the single address encodes, but does not attribute the decoding or determination of the location of the addressed module to the network interface. Besides, the patent application only discloses that the address translation is performed by the address translation means (see p. 9 l. 6-8 of the patent application). This is arranged in the network interface. However, determining the location of the addressed module (feature 6) is not the same as address translation which is performed when arranging first and second information as a single address, but is a subsequent step. Furthermore, the network interface is not identical to the address translation means, but goes beyond it. The address translation means is only part of the network interface.

175 As a result, the patent application does not directly and unambiguously disclose, either explicitly that the network interface determines the selected location of the addressed module within the meaning feature 6. In this regard, the subject matter of claim 1 is inadmissibly extended.

II. Inadmissible extension of the subject-matter of claim 5 as filed

The patent-in-suit as filed is also inadmissibly extended with regard to its claim 5. Since claim 5 as filed, like claim 1, contains at least feature group 3 ("a network interface (ANIP, PNIP) coupled between one of the modules (M, S) and the network (N)"), its subject matter extends beyond the content of the patent application. Reference is made to the explanations regarding claim 1.

III. Auxiliary requests

176 The patent-in-suit cannot be upheld in any amended form according to one of the auxiliary requests.

177 Independent claim 1 of all auxiliary requests contains feature group 3 ("at least one network interface means (ANIP, PNIP) coupled between one of the modules (M, S) and the network [on chip]") and feature 6 ("the network interface determines the selected location of the addressed module (S)"). Therefore, its subject matter goes beyond the content of the patent application.

178 Independent claim 5 of the auxiliary requests 1 and 2 and independent claim 4 of the auxiliary requests 3 and 4 also include feature group 3 and therefore also suffer from added matter.

179 Because, as a result, the independent claims of the patent-in-suit are also affected by the inadmissible extension, the patent-in-suit is to be revoked in its entirety.

C Infringement action

180 The Infringement action is unfounded.

181 The Infringement action is not successful as the patent-in-suit is not valid (see above). In addition, the attacked embodiment does not realise the technical teaching of claim 1 of the patent-in-suit, which is therefore not infringed.

I. Attacked embodiment

182 All Qualcomm NoC ICs having NoC interconnects that the Claimant alleges to be Arteris NoC, i.e. that they contain a NoC designed using tools of the company Arteris Inc. and/or derivatives thereof, are the attacked embodiment (hereinafter: the attacked embodiment).

1. Legal principles

183 It is the Claimant who determines in the Statement of Claim which situation and circumstances the Court is to decide on in terms of location, time and substance. The underlying facts form the basis for the Court's decision and at the same time limit the court's competence to decide. In the event of a patent infringement action, the facts which are particularly relevant are those that allegedly constitute patent infringement within the meaning of Art. 25 ff. UPCA and fulfil the requirements for Court measures pursuant to Art. 56 ff. UPCA. Of particular importance in this context, beside the infringing act, is the design of a product or process as alleged by the Claimant, which, according to the Claimant's submission, is said to comprise all the features

of the asserted patent claim. This essentially represents the "attacked embodiment." Accordingly, the "attacked embodiment" is regularly determined by the factual design of a certain product or a process with regard to the features of the invoked patent claim as asserted in the Statement of Claim. This can be a specific product determined, for example, by its product name, product sheet and technical design. However, the attacked embodiment may also comprise all products that generally have the technical features specified by the Claimant, which allegedly realise the technical teaching of the patent claim. This may also include products unknown to the Claimant or, in the case of an injunction, future products insofar as they essentially correspond to the features of the product presented by the Claimant in his Statement of Claim, which he considers decisive for the patent infringement. In such a case, it is usually sufficient if the Claimant has exemplified the infringement on a sample of the attacked embodiment. What is ultimately meant by the attacked embodiment depends on the interpretation of the Claimant's submission. Once this has been defined it is for the Court to decide whether this attacked embodiment realises the teaching of the patent claim.

2. <u>Case at hand</u>

184 In the present case, the attacked embodiment is not only limited to the specific processor Snapdragon 8+ Gen. 1 but comprises all Qualcomm NoC ICs having NoC interconnects that the Claimant alleges to be Arteris NoC, i.e. include a NoC designed using tools of the company Arteris Inc. and/or derivatives thereof. The Claimant clearly states in its Statement of Claim that it is attacking products

> "that include ICs that incorporate, implement, utilize, include, or otherwise comprise NoCs designed using tools from the company Arteris Inc. ('Arteris NoC') or NoCs which are materially similar (core-identical) to such Arteris NoCs. These products are patent infringing 'infringing embodiments'." (p. 39 of the Statement of Claim)

On the preceding pages of the Statement of Claim, the Claimant has explained what it means by "NoCs designed using tools from the company Arteris Inc." According to this, all attacked embodiments (in the Claimant's own words: "infringing embodiments") comprise integrated circuits (ICs) of the Defendants, having network on chip (NoC) interconnects (these are the "Qualcomm NoC ICs"). These ICs include SoCs, such as Snapdragon 8+ Gen. 1. The Qualcomm NoC ICs comprise a network as on-chip interconnect. More particularly, the network concerns a network on chip (NoC). These NoCs include (but are not limited to) a NoC designed using tools of the company Arteris and/or derivatives thereof (these are the "Arteris NoC"). For the meaning of "Arteris NoC", the Claimant refers to Arteris NoC Chapter submitted as Exhibit P 11. Consequently, the attacked embodiment covers all products that feature NoC which, according to the Claimant's submission, are designed in accordance with the Arteris NoC Chapter. In this context, the mention of the Snapdragon 8+ Gen. 1 has only been made by way of example.

185 This is also clear from the fact, that, with regard to the list of specific processors and other products provided in the Statement of Claim (see p. 43 ff. of the Statement of Claim), the Claimant refers to "non-limiting examples of infringing embodiments" (p. 43 of the Statement of Claim). This shows that the attacked embodiment is not limited to the Snapdragon 8+ Gen. 1 or products expressly listed in the Statement of Claim but comprises all products in the meaning of the general definition put forward by the Claimant. The Snapdragon 8+ Gen. 1 is only the model that exemplifies the attacked embodiment and on the basis of which the Claimant attempts to demonstrate infringement of the patent-in-suit.

186 It follows from this, that the attacked embodiment in any case covers all of the Defendants' products listed in the Statement of Claim, but is not limited to them. The single exception is the processor MSM6000, which the Defendants contest as falling within the Claimant's definition of the attacked embodiment as it uses a different technology than the processor Snapdragon 8+ Gen. 1 and does not even have a NoC. The Defendants have not disputed that other processors fall within the scope of the definition of the attacked embodiment. In this respect, the Claimant's simple assertion that all the other listed models are corresponding processors is sufficient. It would have been incumbent on the Defendants to dispute this for certain models on the list. This is reasonable for them because they know their own products best. Instead, however, they have merely made unsubstantiated claims that there were other models on the list which were already publicly available before the priority date of the patent-in-suit without using any NoC technology. This is not sufficient to dispute the Claimants' assertion.

187 The Samsung Galaxy smartphones, chromebooks, laptops and tablets, which the Claimant refers to as "infringing embodiments IV" by the Claimant, do not constitute a further attacked embodiment. Since they contain processors that constitute the attacked embodiment they do not differ from the attacked embodiment in technical terms or in terms of the features relevant to the realisation of claim 1 of the patent-in-suit. Rather, the arrangement of these processors in electronic devices and the offering and distributing of these devices by companies other than the Defendants raises questions with regard to the infringing acts and the perpetration and participation in such acts.

II. Realisation of claim features

188 It cannot be established that the attacked embodiment makes use of the teaching of claim 1 of the patent in suit.

1. Claimant's assertion of use of Arteris NoC in attacked embodiments

189 The Claimant's assertion that the attacked embodiments comprise NoCs designed using tools developed by Arteris and described in the Arteris NoC Chapter (Exhibit P 11), in particular using the Danube IP library, is unsubstantiated and does not contain any facts that conclusively indicate how the attacked embodiment functions. The Defendants have

substantively contested the use of Arteris NoC and tools described in the Arteris NoC Chapter by explaining the functioning of the attacked embodiments and demonstrating that the attacked embodiment does not implement all the features of claim 1 of the patent-in-suit. The Claimant has not put forward any new facts to support its assertions.

a) Statements of the Claimant

190 The Claimant has relied its assertions on several statements of Arteris and third parties in the past. According to this, the Defendants have been using Arteris NoC technology for over a decade. Arteris states on its website that "Arteris-developed NoC technology is the backbone of Snapdragon application processors & LTE modems, Atheros wireless connectivity SoCs, and SCR IoT products." Furthermore, the Defendant 4) hired approximately 43 Arteris engineers and acquired certain Arteris SoC technology and IP in 2013, licensed such SoC technology and IP back to Arteris, and provides improvements to, and engineering support for, such SoC technology and IP to Arteris.

191 These statements do not reveal which specific technology is used by the Defendants in the attacked embodiment. The underlying facts do not relate to any details of the technology used. While FlexNoC is mentioned in connection with the acquisition of Arteris technology, no further information about this technology is provided, nor has the Claimant submitted any further details on this matter. In particular, the Claimant has not stated nor is it otherwise apparent, that FlexNoC technology is used by the attacked embodiment and corresponds to or at least encompasses the Arteris NoC technology described in the Arteris NoC Chapter. The book "Networks-On-Chips Theory and Practice", including the Arteris NoC Chapter, was published in 2009 (see Exhibit P 11). Defendant 4) hired Arteris's 43 employees and acquired Arteris' technology in 2013. It cannot be ruled out that Arteris had other NoC applications at its disposal in addition to the technology described in the Arteris NoC chapter and that Defendant 4) acquired a different technology. Nor can it be ruled out that Arteris further developed its technology between 2009 and 2013 and that the technology sold differs in relevant respects from the technology described in the Arteris NoC Chapter. It is also possible that the defendants further developed the acquired technology and that the functionality of the attacked embodiments differs significantly from that of the Arteris NoC Chapter. In this context, the Defendants have pointed out that the Arteris NoC technology presented in the Arteris NoC Chapter is presumably a proprietary Arteris technology. Accordingly, the authors of this Chapter also describe this technology as a complete commercial solution for SoC communication architecture of Arteris company (p. 311 of Exhibit P 11). It cannot be assumed that the Defendants simply adopted this commonly known technology identically several years later and maintained it for a decade without amendments. There is therefore no indication that the Defendants are using precisely the technology described in the Arteris NoC Chapter, at least not the parts relevant for the realisation of the claim features. For the reasons mentioned above, this seems rather precluded.

b) <u>Statements of the Defendants</u>

192 The Defendants have expressly disputed that the attacked embodiment was designed identical to Arteris NoCs described in the Arteris NoC Chapter; the Arteris NoC Chapter does not describe NoCs on Qualcomm chips. Above all, the Defendants have stated and confirmed in a written witness statement of ████████████, former Arteris employee and with Qualcomm since 2013, now responsible for the team that manages the technology used for designing NoC, that Qualcomm's design tool does not comprise the Danube NoC IP block library, i.e. the basis for the Arteris solution for SoC communication architecture (p. 311 Exhibit P 11), and none of the NoCs designed with the proprietary Qualcomm NoC design tool uses the NTTP packet structure as shown in the Arteris NoC Chapter (Exhibit BP 3).

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c) <u>Result</u>

194 As the Claimant has not presented any substantiated facts which establish a different functioning of the attacked embodiment than that specified by the Defendants, its assertion that the attacked embodiment makes use of Arteris NoC technology as described in the Arteris NoC Chapter is already inconclusive and therefore not suitable to establish the realisation of the technical teaching of claim 1 of the patent-in-suit.

2. <u>No realisation of all claim features based on Defendants' submissions</u>

195 Furthermore, it is apparent from the Defendants' statement on the functioning of the attacked embodiment that the device does not implement all the features of claim 1.

a) Feature groups 1 to 3

196 It can remain open whether the contested embodiment implements the feature groups 1 to 3.

197 The Claimant has pointed out that it can be inferred from the Defendant's submission that the attacked embodiment performs address mapping as described in the patent specification. Such an address mapping also corresponds to feature groups 1 to 3.

198 Features 1 to 2.2 and feature group 3 are indisputably realised in any case. However, the implementation of features 2.2.1 and 2.2.2 in the attacked embodiment can also not precluded. Based on the claim construction as set out above, feature group 2.2 only requires that a first information indicative for a location of an addressed module within the network and a second information indicative for a location within the addressed module can be derived from the message issued by the first module through calculation, translation, interpretation or other means of decoding. ████████████████████████████████████ ████████████████████████████████████ and the message finds its location within the addressed module, it does not appear to be excluded that information according to feature group 2.2 can also be derived from the message issued by the first module, in particular from the address taken from the overall system memory map. The Defendants' denial of feature 2.2 is based solely on a different claim interpretation, which, however, cannot be accepted. The same applies to the interpretation of the expression "module within the network". The modules of the attacked embodiment are not part of the network, however, they can be addressed via the network.

199 Ultimately, all this can be left open as at least claim features 4.2, 5 and 6 are not implemented in the attacked embodiment.

b) Feature 4.2

200 The Defendants do not dispute that the NIUs of the attacked embodiment contain a type of address translation means. The logic within the NIU, which determines the route for the message to the NIU associated with the target module based on the address provided by the first module, can be regarded as an address translation means arranged in an interface means within the meaning of claim features 4 and 4.1.

201 However, this address translation means is not capable of arranging the first and second information as a single address, as required by feature 4.2 of claim 1. According to the Defendants' explanations of the attacked embodiment, ████████████████████ ████████████████████████████████████ ████████████████████████████████████ ████████████████████████████████████ ████████████████████████████████████ ████████████████████████████████████ ████████████████████████████████████

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██████████████████████████████████. The Defendants expressly state that this route or path information does not contain any information about which module is addressed and about a location within the addressed module, but only the path information to the network interface connected to the addressed module, since the route only guides the packet up to the network interface of the addressed module.

202 The route resp. path information cannot be regarded as first and second information arranged in a single address within the meaning of claim feature 4.2. The Defendants rightly point out that, in accordance with the patent description (para. [0031]), an address can be decoded to find a route, but a route does not constitute an address. ███████████████████████

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██████████, there is also no information indicative for a location of an addressed module within the network or for a location within the addressed module. The exit port of the switch does not provide any indication of the location of the addressed module, let alone a location within the addressed module.

c) <u>Features 5 and 6</u>

203 Even if one assumes that feature group 4 is implemented because the mapping of the address supplied by the first module to path information in the table is considered to be an arrangement of the first and second information as a single address within the meaning of feature 4.2, the contested embodiment does not realise features 5 and 6. It has not been argued by the Claimant, nor is it apparent, how the two further steps of determining the module and its location based on the single address are to be carried out or by what process these steps are to be realised. Rather, such steps do not even seem to be necessary.

204 The Defendants expressly state that ███████████████████████████████

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██████████████████████████████████. According to this explanation, there is no step of determining the addressed module or the location of the addressed module based on the single address. ████████████████████████

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██████████████████████, it cannot be assumed that the addressed module and the location of this module will also be determined, and that this will be done based on the address containing the path information.

205 The Claimants argument that the addressed module is determined ███████████████

██████████████████████████████████████, cannot be accepted. The step of determining the addressed module necessarily follows the step of arranging of first and second information in the single address, because the determination is based on the single

address. However, if the step of determining the route for the NIU associated with the target module is regarded as arranging the information as a single address, it cannot simultaneously be the step of determining the addressed module. As explained in the context of claim construction, these are different steps that must be performed sequentially. However, with regard to the attacked embodiment, once the route has been determined, there is no second or third step (of determining whatever). The path information is the immediate basis for forwarding the message. The same applies to feature 6 and the Claimant's argument that determining the selected location of the addressed module would be the core principle of memory mapping. However, this argument does not deal with the details of the functioning of the attacked embodiment.

3. No realisation of all claim features based on Arteris NoC chapter

206 Notwithstanding the fact that the Claimant has not conclusively stated that the attacked embodiment is designed using tools developed by Arteris and described in the Arteris NoC Chapter, it cannot even be established that an embodiment corresponding to the Arteris NoC Chapter makes use of the teaching of claim 1 of the patent-in-suit. Features 5 and 6 are not realised.

207 If it is assumed that the packet header and the necker cells containing the Master Address, the Slave Address and the Slave offset according to the Arteris NoC Chapter (Fig. 11.2 and section 11.3.1.2 of Exhibit P 11, see below) correspond to first and second information within the meaning of feature group 2.2 and even if the translation of AHB transactions into an equivalent NTTP packet sequence with packet header and necker cells according to the Arteris NoC Chapter (section 11.3.2.1 of Exhibit P 11) is regarded as arranging the first and the second information in a single address within the meaning of feature 4.2, it is nevertheless not argued, nor is it apparent, that, based on this single address (header and necker of the NTTP sequence), the addressed module and the selected location of this module is determined or at least that the attacked embodiment is adapted to do so.
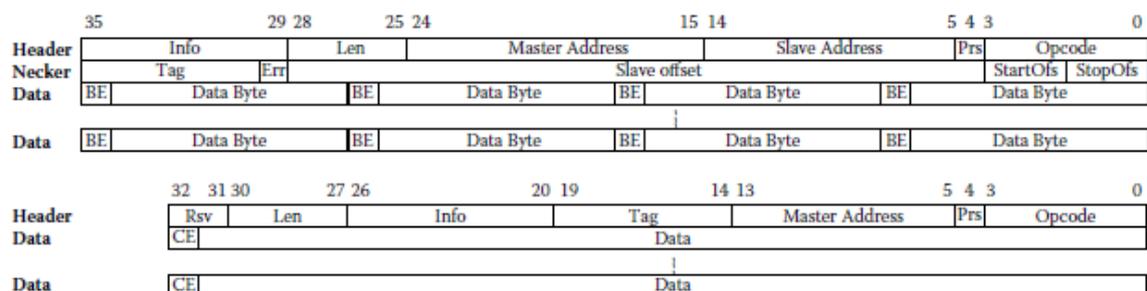
	35	29 28	25 24	15 14	5 4 3	0
Header	Info	Len	Master Address	Slave Address	Prs	Opcode
Necker	Tag	Err	Slave offset		StartOfs	StopOfs
Data	BE Data Byte	BE Data Byte	BE Data Byte	BE Data Byte		
Data	BE Data Byte	BE Data Byte	BE Data Byte	BE Data Byte		

	32 31 30	27 26	20 19	14 13	5 4 3	0
Header	Rsv Len	Info	Tag	Master Address	Prs	Opcode
Data	CE	Data				
Data	CE	Data				

FIGURE 11.2
NTTP packet structure.

208 The Arteris NoC Chapter itself is silent on such further steps, and they cannot be inferred from it either.

209 The Claimant refers to section 11.3.2.1 of the Arteris NoC Chapter which inter alia reads:

"The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size."

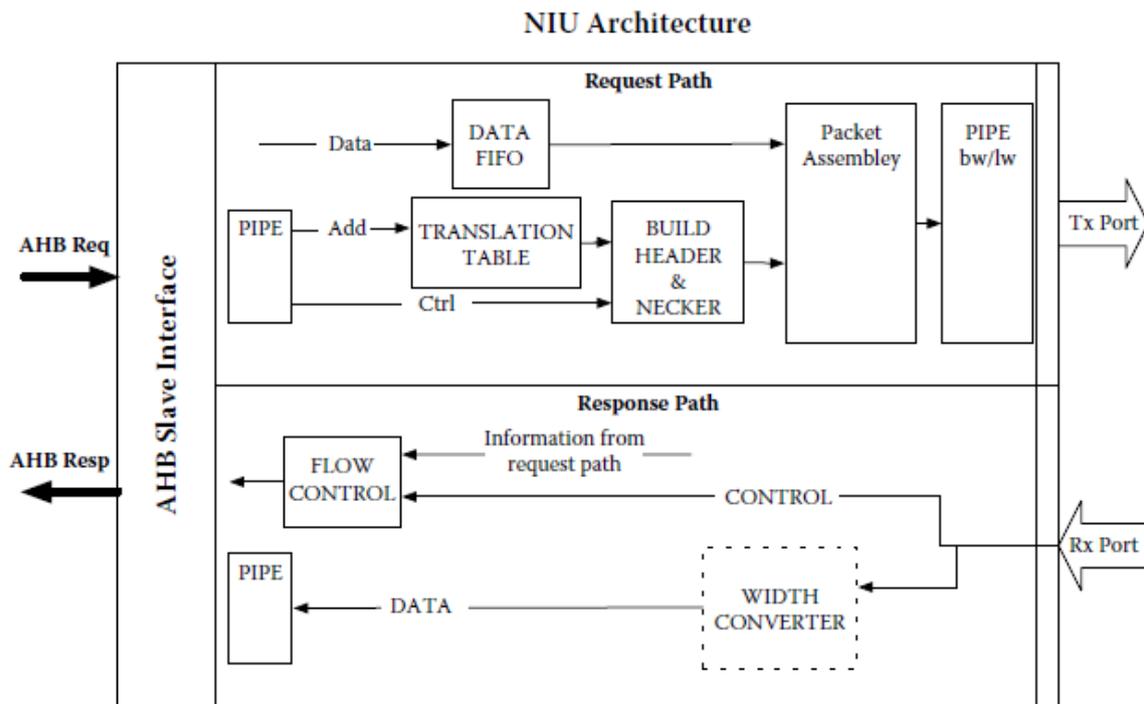210 This is also depicted in the following Figure 11.4 of the Arteris NoC Chapter:

NIU Architecture

FIGURE 11.4
Network interface unit: Initiator architecture.

211 However, it cannot be inferred from the phrase "[the packet header and necker information] is needed to access the NTTP address space" that the address translation means resp. network interface is also adapted to determine the addressed module and its location based on this information. The term "NTTP address space" only describes the space in which the NTTP protocol is applicable. This does not preclude that router and switches of the network directly act upon the header and necker information contained in the NTTP sequence and a further step of determining the addressed module and its location is not required. At least, Figure 11.4 in the Arteris NoC Chapter does not show that the NIU performs any further step after building the header and necker and after packet assembly. Instead, the NTTP sequence is transferred to the TX Port.

212 In this context, the Claimant only states that, "in other words, the single address allows to determine the addressed location in the NTTP address space, which requires knowledge

about which slave is addressed/about the selected location of the slave." However, it is not argued, nor is it apparent, that the addressed module or its location is actually determined or the NIU is adapted to do so. Rather, the Header and Necker already contain the Master Address and Slave Address, so that the determination of the addressed module and its location by the address translation means or the NIU does not even seem necessary.

213 The same applies as far as the Claimant refers to the following passage in section 11.3.1.2 of the Arteris NoC Chapter:

"The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. (…) the necker, in the request packet to provide detailed addressing information to the target."

This does not imply that the address translation means determines or can determine the addressed module or its location based on the NTTP sequence, i.e. the single address. It is not precluded that this information is only used by the network routers and switches.

214 Finally, the Claimant refers to the target NIU and the explanation in section 11.3.2.2 of the Arteris NoC Chapter:

"For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable."

This does not imply that the NIU determines or can determine the addressed module or its location based on the NTTP sequence. Instead, the slave offset, the start/stop offset, and the slave address fields are only used for mapping the AHB address space from the NTTP address space. The Arteris NoC Chapter is silent on whether the addressed module and/or its location is determined. Actually, this would not be necessary as the addressed NIU is directly associated with the target module.

215 As a result, the Claimant's submissions are inconclusive.

4. Application to produce evidence

216 It follows from the reasons stated above that the Claimant's application to produce evidence is not successful and must be rejected.

a) Parties' submissions

217 The Claimant is of the opinion that it has described and substantiated the patent infringement in detail. The outline of infringement is based on the fact that the design of the Defendants' NoC ICs equals the Arteris NOC technology described in Arteris NoC Chapter. It is undisputed

that the Defendants have used Arteris technology in their infringing embodiments for over a decade and the Defendant 4) hired approximately 43 Arteris engineers and acquired certain Arteris SoC technology and IP in 2013. However, Defendants stated that the Arteris NoC chapter does not fully describe the NoCs on the Defendants' infringing embodiments and claim that the details of the Arteris NoC technology differs from the design used for the Qualcomm NoCs. The Claimant argues that the Defendants should be ordered to produce evidence, in particular the source code and the technical documents of the infringing embodiments, since Claimant has presented the Arteris NoC Chapter as evidence in support of its claims and does not have access to any other available evidence whereas the Defendants know and have access to these documents, as these have already been produced by the Defendants in the parallel US proceedings pending with the Western District of Texas.

218 The <u>Defendants</u> argue that the Claimant has not sufficiently specified any evidence to be produced. The sheer volume of data related to the source code already shows that Claimant's request is not aimed at obtaining specific evidence for showing the use of a certain claim feature, but a comprehensive US style discovery, a so-called "fishing expedition", which Rule 190 RoP does not support. Furthermore, Claimant has not specified which facts should be evidenced by the requested information. Finally, the Claimant has failed to show that the evidence to be produced by Defendants serves to substantiate the alleged infringement claim. In the Defendants' view, the Claimant has not even presented its infringement claim conclusively.

b) <u>Requests</u>

219 Originally, the Claimant requested, that the Defendants 3), 4) and 5) are ordered to produce the source code and the internal and external technical documents of (I.) the System on Chip (SoC) architecture of the infringing embodiments, (II.) the infringing embodiments, evidencing the communication between the processing modules through the NoC interconnect, and (III.) the infringing embodiments, evidencing how Quality of Service (QoS) is supported and managed in Defendants NoC infrastructure.

220 Later, the Claimant has amended its application and now requests:

 I. The so-called "Qualcomm source code" which is specifically identified and individually addressed in the Western District of Texas Action Order dd. 26 November 2024 – see Network System Technologies, LLC v. Qualcomm Inc. et al., Case No. 1:22-cv-1331-DAE, Dkt. 259, – whereas the evidence production may be performed by (1) producing to Claimant the paper printouts of the source code already generated and provided to Claimant in the Western District of Texas WDTex Action, and by (2) allowing Claimant's party expert ▮▮▮▮▮▮▮ access to the aforesaid "Qualcomm source code" and access to these paper printouts, and by disclosing the "Qualcomm source code" to him again at the premises of ProSearch's Secure Facility, located at 3250 Wilshire Blvd., Los

Angeles, CA 90010, USA, where it is currently stored and displayed for the purpose of production of evidence in the Western District of Texas Action, and by allowing Claimant's party expert ██████████ to document and to describe the "Qualcomm source code", for example, by taking and making written notes and requesting printouts;

II. The so-called "NST supplemental infringement contentions" which are specifically identified and individually addressed in the Western District of Texas Action Order dd. 26 November 2024 and that were amended by Claimant on 7 February 2025, as stated in Claimant's Notice of Compliance – see Network System Technologies, LLC v. Qualcomm Inc. et al, Case No. 1:22-cv-1331-DAE, Dkt. 292; and

III. The "documents" which are specifically identified and individually addressed by Claimant in Claimant's 7 February 2025 "NST supplemental infringement contentions" – see Network System Technologies, LLC v. Qualcomm Inc. et al, Case No. 1:22-cv-1331-DAE, Dkt. 292.

221 The Defendants request that

Claimant's "Amendment of Request pursuant to R. 190 RoP" be dismissed.

c) <u>Grounds for rejection</u>

222 The Claimant's request for an order to produce evidence has no basis in Art. 59 (1) UPCA and Rule 190.1 RoP and is therefore unfounded.

(1)

223 According to Art. 59 (1) UPCA and Rule 190.1 RoP, the Court may, where a party has presented reasonably available and plausible evidence in support of its claims and has, in substantiating those claims, specified evidence which lies in the control of the other party or a third party, on a reasoned request by the party specifying such evidence, order that other party or third party to produce such evidence. For the protection of confidential information, the Court may order that the evidence be disclosed to certain named persons only and be subject to appropriate terms of non-disclosure.

224 In accordance with the case law of the Court of Appeal ("CoA") of the UPC, as also adopted by different Local Divisions, the following principles apply to a request under Rule 190 RoP.

225 As a rule, an order to produce evidence presupposes that there is a fact that is relevant to the substantiation of claims (or defences) and that the fact requires proof by the party who is making the application (also cf. the CoA referred to above, para. 36, explaining that the purpose of these provisions is to ensure that the party who has the burden of proof will have access to the tools for carrying this burden). To this end, the applicant must set out in the

application which fact it wishes to prove by which means of evidence and for what reason. No evidence is required for a fact that is not (specifically) contested (see Rule 171.2 RoP). If a fact is not relevant to the claims (or defences) being pursued, ordering the production of evidence for such a fact is generally at least disproportionate (CoA, Order of 24 September 2024, UPC_CoA_298/2024 – Panasonic/Oppo; LD Mannheim, Order of 20 October 2024, UPC_CFI_471/2023 – Dish/Aylo; LD Munich, Order of 3 April 2025, UPC_CFI_846/2024 – Promosome/BionTech).

226 An applicant for an order pursuant to Rule 190 RoP must have presented reasonably available and plausible evidence in support of its claims (or defences) before an application under Rule 190 RoP can be granted. Whether the applicant has met this requirement and, as a result, whether an order to evidence against the opponent or a third party can be considered is at the discretion of the Court. When exercising this discretion, the circumstances of the individual case must be taken into account, taking into account the mutual interests and the principle of efficient conduct of proceedings (CoA, Order of 24 September 2024, UPC_CoA_298/2024 – Panasonic/Oppo; LD Mannheim, Order of 20 October 2024, UPC_CFI_471/2023 – Dish/Aylo; LD Munich, Order of 3 April 2025, UPC_CFI_846/2024 – Promosome/BionTech).

227 The burden of presentation and proof for the existence of the prerequisites for an order to produce evidence, lies with the applicant (CoA, Order of 24 September 2024, UPC_CoA_298/2024 – Panasonic/Oppo; LD Mannheim, Order of 20 October 2024, UPC_CFI_471/2023 – Dish/Aylo; LD Munich, Order of 3 April 2025, UPC_CFI_846/2024 – Promosome/BionTech).

(2)

228 Applying the above principles to the present case, the Court exercises its discretion not to issue an order to produce evidence. The Claimant's requests are not well-founded.

229 The Claimant has already failed to present any plausible evidence to support its claim. The allegation of the infringement of the patent-in-suit is based solely on the Arteris NoC Chapter and the fact that the Defendants have acquired Arteris technology and have been using it for some time. However, the Arteris NoC chapter does not constitute plausible evidence for the Claimant's assertion. As already mentioned, the Arteris NoC chapter does not constitute conclusive evidence of infringement. Even if one were to assume that only individual features cannot be proven, it must be taken into account that the Claimant based its case from the outset on the Arteris NoC chapter and the assertion that this proves the infringement of the patent-in-suit. In doing so, the Claimant could not even assume that the Arteris NoC chapter describes the functionality of the attacked embodiment because the Arteris NoC Chapter does not originate from the Defendants nor does it refer to the Defendants' ICs and chips. The Claimant concludes that the technology described in the Arteris NOC Chapter is used solely because there have been connections between Arteris and the Defendants in the past (acquisition of technology, takeover of employees and the like). From a technical point of view, this is completely unspecific for the infringement of the patent-in-suit. The Claimant could not assume that the Arteris technology Defendants acquired was identical to the details described

in the Arteris NoC Chapter. Rather, it can be presumed that, as the Defendants also argue, Arteris and the Defendants each use proprietary technology that differs in key aspects.

230 Furthermore, the Defendants also disputed the use of the technology according to the Arteris NoC Chapter and even explained the different mode of operation. Only then did the claimant request the submission of the source code. At that time, and even now, the Arteris NoC Chapter appears completely implausible, also in view of the Defendants' submissions. The Claimant entered the proceedings on the basis of the Arteris NoC Chapter with a mere assumption about the functionality of the attacked embodiment, and this assumption proved to be untenable. There is more to suggest that request for the production of the source code only serves to find a new justification for the infringement claim or ultimately confirms the Defendant's submission. However, an order to produce evidence pursuant to Rule 190.1 RoP does not serve this purpose. It already lacks a plausible evidence in support of Claimant's claim.

231 The application to produce evidence is ultimately aimed at finding out how the attacked chips possibly work. Based on claim 1 of the patent in suit, the Claimant does not specify any individual features or functionalities of the chips that are still missing for the purpose of proving patent infringement and for which specific evidence is to be presented. The sheer volume of documents that are the subject of the application for production of evidence indicates that the allegation of infringement was made completely in the dark and that the application was filed in the hope of finding any evidence of a possible infringement. This is further indicated by the fact that the application does not differ in any way from the applications in the parallel proceedings, even though different technologies are involved.

232 Against this background, the requested order cannot be granted. This is without even taking into account the fact that the source code to be inspected contains highly sensitive technical trade secrets of the Defendants, the disclosure of which should not be ordered without good reason, even taking into account possible confidentiality measures.

233 The Claimant's statement during the oral hearing that this is a classic case for the submission of the source code in accordance with Rule 190 of the RoP cannot be accepted for the reasons stated above. For these reasons, the witnesses offered by the Claimant were also not heard. The Claimant's objection that the Defendants only presented a written witness statement and that the witness was not heard at all is not valid. The Claimant bears the burden of proof for the alleged infringement and has not presented its claim in a conclusive manner. In this respect, the mere dispute by the Defendants was sufficient.

234 Insofar as the Claimant indicated in the oral hearing that the request for the production of evidence could have been decided earlier and, in any case, instructions could have been given if there was a lack of plausible evidence, this cannot be accepted. In the present case, a decision on the application under Rule 190 RoP could only be made after comprehensive preparation of the case. If a production of evidence had been considered, the hearing could

have been adjourned or reopened. However, even in the oral hearing, the Claimant did not present any further possible evidence to substantiate its claim.

<u>DECISION</u>

1. The European patent EP 1 552 669 is revoked with effect to the territories of France (FR) and Germany (DE).

2. The Application to amend the patent in suit is dismissed.

3. The Infringement action is dismissed.

4. The costs of the Infringement action against the Defendants 3) to 5) and the costs of the Counterclaim for revocation are to be borne by the Claimant.

5. The value in dispute for the Infringement action is set at EUR 3,000,000. The value in dispute for the Counterclaim for revocation is set at EUR 4,500,000.

On behalf of the Presiding Judge Ulrike Voß, in her absence: Daniel Voß (Legally Qualified Judge)	
Daniel Voß (Legally Qualified Judge)	
Pierluigi Perrotti (Legally Qualified Judge)	
Andrea Scilletta (Technically Qualified Judge)	
For the sub-registrar	

<u>INFORMATION ON APPEAL</u>

An appeal against this decision may be brought before the Court of Appeal by any party whose claims have been unsuccessful, in whole or in part, within two months of service of the decision (Art. 73(1) UPCA, R. 220.1 (a) RoP, 224.1 (a) RoP).

<u>INFORMATION ON ENFORCEMENT (ART. 82 UPCA, ART. 37(2) UPCS, R. 118.8, 158.2, 354, 355.4 RoP)</u>

An authentic copy of the enforceable order will be issued by the Deputy-Registrar upon request of the enforcing party, R. 69 RegR.

<u>INSTRUCTION TO THE REGISTRY</u>

A certified copy of the decision shall be sent to the European Patent Office and the national Patent and Trademark offices as soon as the decision on the revocation action has become legally binding.

This decision was read in open court on 11 March 2026.

<u>Note</u>

This document is a redacted version of the Decision, with confidential information removed. It is valid without the signatures of the judges involved and the representative of the Sub-Registrar.

Daniel Voß

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