Local Division Munich

UPC_CFI_64/2024

UPC_CFI_450/2024

Decision

of the Court of First Instance of the Unified Patent Court
Local Division Munich
delivered on 11 March 2026

HEADNOTES

The “attacked embodiment” is regularly determined by the factual design of a certain product or a process with regard to the features of the invoked patent claim as asserted in the Statement of Claim. This can be a specific product determined, for example, by its product name, product sheet and technical design. However, the attacked embodiment may also comprise all products that generally have the technical features specified by the Claimant, which allegedly realise the technical teaching of the patent claim. This may also include products unknown to the Claimant or, in the case of an injunction, future products insofar as they essentially correspond to the features of the product presented by the Claimant in his Statement of Claim, which he considers decisive for the patent infringement. In such a case, it is usually sufficient if the Claimant has exemplified the infringement on a sample of the attacked embodiment.

CLAIMANT AND COUNTERDEFENDANT

Network System Technologies LLC, legally represented by its Chief Executive Officer (CEO) Warren Hurwitz,533 Congress Street, Portland, ME 04101, United States of America,

represented by: Dr. Thomas Gniadek, Hoffmann Eitle Patent- und Rechtsanwälte PartmbB, Arabellastraße 30, 81925 Munich.

DEFENDANTS AND COUNTERCLAIMANTS

3. **Qualcomm Incorporated**, legally represented by its Chief Executive Officer (CEO) Cristiano Amon, 5775 Morehouse Drive, San Diego, CA 92121, United States of America,

4. **Qualcomm Technologies, Inc.**, legally represented by its Chief Executive Officer (CEO) Cristiano Amon, 5775 Morehouse Drive, San Diego, CA 92121, United States of America,

5. **Qualcomm Germany GmbH**, legally represented by its Chief Executive Officer (CEO) Hamid-Reza Nazeman, Anzinger Straße 13, 81671 Munich, Germany,

represented by: Johannes Heselberger, Bardehle Pagenberg Partnerschaft mbB, Prinzregentenplatz 7, 81675 Munich.

PATENT AT ISSUE

European Patent n° EP 1 875 683

PANEL/DIVISION

Panel 2 of the Local Division Munich

DECIDING JUDGE/S

This decision has been issued by Presiding Judge U. Voß, legally qualified Judge D. Voß (Judge-rapporteur), legally qualified Judge P. Perrotti and technically qualified Judge A. Scilletta

LANGUAGE OF THE PROCEEDINGS

English

SUBJECT-MATTER OF THE PROCEEDINGS

Infringement action and Counterclaim for revocation

DATE OF ORAL HEARING

16 December 2025

SUMMARY OF FACTS

1 The subject matter of these proceedings is an Infringement action brought by the Claimant against the Defendants 3) to 5) and a Counterclaim for revocation brought by the Defendants 3) to 5) (hereinafter: Defendants). The proceedings are part of an international patent dispute between the Claimant and the Defendants. Claimant has also filed a U.S. civil action in the United States District Court for the Western District of Texas (Austin Division), Civil Action No. 1:22-cv-1331 against the Defendants 3) and 4) and Arteris, Inc.

2 Originally, the Claimant also sued Samsung Electronics Co., Ltd. and Samsung Semiconductor Europe GmbH (Defendants 1) and 2)), two companies belonging to the Samsung Group, which also filed a Counterclaim for revocation. On 6 September 2024, at request of the Claimant and the Defendants 1) and 2), the Court permitted the withdrawal of the Infringement action and the Counterclaim for revocation in relation to Defendants 1) and 2) respectively.

3 The basis for the present Infringement action and the object of the related Counterclaim for revocation is the European Patent EP 1 875 683 (Exhibit P 1; hereinafter: patent-in-suit) regarding an integrated circuit (IC) with data communication network and an integrated circuit design method. The application of the patent-in-suit was filed by Koninklijke Philips Electronics N.V. on 20 April 2006, claiming priority of the European application No. 5103232 dated 21 April 2005. The application was published on 9 January 2008, the mention of the grant of the patent-in-suit on 7 September 2011. The patent-in-suit was validated in a number of jurisdictions including France and Germany, where it is still in force. The patent-in-suit was opted out of the competence of the UPC on 25 May 2023, but this opt-out was subsequently withdrawn on 20 December 2023. A preliminary objection based on the allegedly invalid withdrawal of the opt-out was rejected by order dated 25 August 2025.

4 Claimant asserts claims 1 and claim 8 of the patent-in-suit which read as follows:

Claim 1:

> “An integrated circuit (10) comprising:
>
> a plurality of functional blocks (101, 102, 103, 104); and
>
> a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional

blocks (101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108), the data communication network (100) comprising a first data router (140) and a second data router (120) interconnected through a first communication channel (150), characterized in that the first communication channel (150) comprises M*N data storage elements (160), M being a positive integer, for delaying whole data packages including the routing information by introducing a delay of M*N cycles on the first communication channel (150)."

Claim 8:

"A method of designing an integrated circuit (10) comprising a plurality of functional blocks (101, 102, 103, 104), and a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface; characterized in that the method comprises:

identifying a first communication channel (150) between a first data router (140) and a second data router (120) that has a data transfer delay exceeding a predefined delay threshold; and

inserting M*N data storage elements (160) into the first communication channel (150), M being a positive integer, for delaying whole data packages including the routing information by introducing a delay of M*N cycles on the first communication channel (150)."

5 Originally, the actual and registered proprietor of the patent-in-suit was Koninklijke Philips Electronics N.V. (hereinafter: "Philips"). On 24 June 2022, the Claimant and Philips concluded a Patent Purchase Agreement ("PPA", submitted as Exhibit P 24) according to which the patent-in-suit and an associated integrated circuits patent portfolio should be transferred from Philips to the Claimant. Corresponding Patent Assignments ("PAs", submitted as Exhibit P 25) covering the French and the German Part of the patent-in-suit were signed on 5 July 2022. Transfer and change of ownership were recorded in the EPO patent register on 8 May 2023

as well as in the national patent registers of France and Germany. An excerpt of these registers has been submitted as Exhibit P 2 – P 5.

6 The Claimant is a patent licensing company that seeks to license the patent-in-suit and the corresponding patent portfolio to semiconductor companies and companies that deploy those semiconductors.

7 Defendant 3) creates and designs semiconductors, software and services related to wireless technology.

8 Defendant 4) is a subsidiary of Defendant 3) and operates, along with its subsidiaries, substantially all of Qualcomm's engineering, research and development functions, and substantially all of their products and services businesses, including the QCT semiconductor business. The product range of Defendant 4) includes, among other things, Snapdragon and Qualcomm branded products.

9 Defendant 5) is a subsidiary of Defendant 3) and Defendant 4).

10 Defendant 3) and Defendant 4) design a variety of products regarding wireless technology, including ICs and especially the Snapdragon SoC family, which is used, for example, in smartphones, laptops, VR devices, automotive etc.

11 Arteris, Inc. is a technology firm developing, inter alia, NoC technology (hereinafter: "Arteris"). According to an Arteris, Inc. press release and other news sources from 2013, Defendant 4) hired approximately 43 Arteris engineers and acquired certain Arteris SoC technology and IP in 2013, licensed such SoC technology and IP back to Arteris, and provided improvements to, and engineering support for, such SoC technology and IP to Arteris.

12 The Claimant is objecting to integrated circuits (ICs) offered and distributed by the Defendants 3) to 5). These ICs including Systems on Chip (SoCs), have Network on Chip (NoC) interconnects (hereinafter: Qualcomm NoC ICs), i.e. they comprise a network as on-chip interconnect. According to the Claimant's submission, these NoCs include (but are not limited to) a NoC designed using tools developed by Arteris and/or derivatives thereof (hereinafter: Arteris NoC). For the further explanation of the Arteris NoC, the Claimant refers to Chapter 11 of the book titled 'Networks-on-Chips Theory and Practice' (submitted as Exhibit P 10; hereinafter: Arteris NoC Chapter).

13 According to this, the Arteris NoC is a network on board of the IC which allows the modules of the IC, also referred to as functional blocks, IP blocks or nodes, to communicate with each other. Network interface units (NIUs) and routers/switches are key components of the Arteris NoC, which also makes use of a specific network protocol called NoC Transaction and Transport Protocol (NTTP) proposed by Arteris. This protocol is packet based and adopts a three-layered approach with transaction, transport and physical layers. It defines the rules and conventions that apply as data is transferred over the network. Requests from a (master)

module are sent through the master NIU to the NoC from which they are routed to the NIU of a (slave) module. Response packets from the (slave) module are delivered vice versa through the slave NIU via the network to the requesting master NIU which forwards them to the (master) module. The NIUs create the packets. They translate between third-party protocols like AHB, OCP and AXI used by the modules and the NTTP protocol. For further details of the Arteris NoC, reference is made to the Arteris NoC chapter (Exhibit P 10).

14 The Claimant refers to Qualcomm NoC ICs that include Arteris NoC as “infringing embodiment II” (whereas the term infringing embodiment I is referred to products of Samsung). The following products of the Defendants 3) and 4) are examples of the infringing embodiments II:

15 The Snapdragon Mobile Processors, Platforms and Modems, including:

- Snapdragon 8 Gen 3
- Snapdragon 8 Gen 2
- Snapdragon 8+ Gen 1
- Snapdragon 8 Gen 1
- Snapdragon 7+ Gen 2
- Snapdragon 7 Gen 1
- Snapdragon 6 Gen 1
- Snapdragon 4 Gen 2
- Snapdragon 4 Gen 1
- Snapdragon S4 Play
- Snapdragon S4 Pro
- Snapdragon S4 Plus
- Snapdragon S4 Prime
- Snapdragon S3
- Snapdragon S2
- Snapdragon S1
- Snapdragon 888+
- Snapdragon 888
- Snapdragon 870
- Snapdragon 865+
- Snapdragon 865
- Snapdragon 860
- Snapdragon 855+
- Snapdragon 855
- Snapdragon 845
- Snapdragon 835
- Snapdragon 821
- Snapdragon 820
- Snapdragon 810
- Snapdragon 808
- Snapdragon 805
- Snapdragon 801
- Snapdragon 800
- Snapdragon 782G
- Snapdragon 782
- Snapdragon 780G
- Snapdragon 780
- Snapdragon 778G+
- Snapdragon 778G
- Snapdragon 768G
- Snapdragon 768
- Snapdragon 765G
- Snapdragon 765
- Snapdragon 750G
- Snapdragon 750
- Snapdragon 732G
- Snapdragon 732
- Snapdragon 730G
- Snapdragon 730
- Snapdragon 720G
- Snapdragon 720
- Snapdragon 712
- Snapdragon 710
- Snapdragon 695
- Snapdragon 690
- Snapdragon 685
- Snapdragon 680
- Snapdragon 678
- Snapdragon 675
- Snapdragon 670
- Snapdragon 665
- Snapdragon 662
- Snapdragon 660
- Snapdragon 652
- Snapdragon 650
- Snapdragon 636
- Snapdragon 632
- Snapdragon 630
- Snapdragon 626
- Snapdragon 625
- Snapdragon 617
- Snapdragon 616
- Snapdragon 615
- Snapdragon 610
- Snapdragon 600
- Snapdragon 480+
- Snapdragon 480
- Snapdragon 460
- Snapdragon 450
- Snapdragon 439
- Snapdragon 435
- Snapdragon 430
- Snapdragon 429
- Snapdragon 427
- Snapdragon 425
- Snapdragon 415
- Snapdragon 412
- Snapdragon 410
- Snapdragon 400
- Snapdragon 215
- Snapdragon 212
- Snapdragon 210
- Snapdragon 208
- Snapdragon 200
- Snapdragon X75
- Snapdragon X72

- Snapdragon X70
- Snapdragon X65
- Snapdragon X60
- Snapdragon X55
- Snapdragon X50
- Snapdragon X35
- Snapdragon X20
- Snapdragon X24
- Snapdragon X16
- Snapdragon X15
- Snapdragon X12
- Snapdragon X7
- Snapdragon X5
- MDM9625
- MDM9615
- MDM9225
- MDM9215
- MDM9600
- MDM8225
- MDM9200
- MDM9207-1
- MDM9206
- MDM8215
- MDM8220
- MDM6600
- MDM8200A
- MDM6270
- MDM6200
- 9205

16 The Snapdragon Mobile Compute Processors, including:

- Snapdragon 835 Mobile PC Platform
- Snapdragon 850 Mobile PC Platform
- Snapdragon 7c Compute Platform
- Snapdragon 7c Gen 2 Compute Platform
- Snapdragon 7c+ Gen 3 Compute Platform
- Snapdragon 8c Compute Platform
- Snapdragon 8cx Compute Platform
- Snapdragon 8cx Gen 2 5G Compute Platform
- Snapdragon 8cx Gen 3 Compute Platform

17 The Snapdragon Wearable Processor, including:

- Snapdragon Wear 1100
- Snapdragon Wear 1200
- Snapdragon Wear 2100
- Snapdragon Wear 2500
- Snapdragon Wear 3100
- Snapdragon Wear 4100
- Snapdragon Wear 4100+
- Snapdragon W5
- Snapdragon W5+ Gen 1

18 The Snapdragon Automotive Processors, including:

- Snapdragon 602A
- Snapdragon 820A
- Snapdragon 855A

19 The Snapdragon Embedded Processors, including:

- Snapdragon 410E
- Snapdragon 600E
- Snapdragon 800
- Snapdragon 810
- Snapdragon 820E

20 The Qualcomm Vision Intelligence Processors, including:

- QSC603
- QSC605

21 The Qualcomm Home Hub and Smart Audio Processors, including:

- APQ8009
- APQ8017
- APQ8053
- QSC403
- QSC404
- QSC405
- QSC407

22 The Qualcomm Extended Reality (XR) Processors, including:

- Snapdragon XR1
- Snapdragon XR2

23 The Qualcomm Gaming Processors, including:

- Snapdragon G3x Gen 1

24 Other Qualcomm Processors, including:

- QSC1100
- QSC6010
- QSC6020
- QSC6030
- QSC6240
- QSC6245-1
- QSC6055
- QSC6065
- QSC6260-1
- QSC6270
- QSC6075
- QSC6085
- MSM6000
- MSM6025
- MSM6050
- MSM6100
- MSM6125
- MSM6150
- MSM6175
- MSM6225
- MSM6250
- MSM6250A
- MSM6245
- MSM6255
- MSM6260
- MSM6275
- MSM6280
- MSM6280A
- MSM6800A
- MSM6575
- MSM6550
- MSM6550A
- MSM6800
- MSM6500
- MSM7200
- MSM7200A
- MSM7201
- MSM7500
- MSM7500A
- MSM7600
- MSM7850
- Qualcomm 205
- Qualcomm 215

25 The Claimant also objects to Samsung Galaxy smartphones, chromebooks, laptops and tablets which contain various models of the “infringing embodiments II” and are offered, imported and sold throughout Europe, inter alia in Germany and France, by the former Defendants 1) and 2). The Claimant designates these products as “infringing embodiment IV” (whereas the term infringing embodiment III referred to products of Samsung containing the infringing embodiment I) and lists the following products as examples for the “infringing embodiment IV”:

26 Samsung Galaxy S-Series smartphones:

- Samsung Galaxy S23 Ultra
- Samsung Galaxy S23 Plus
- Samsung Galaxy S23
- Samsung Galaxy S22 Ultra 5G
- Samsung Galaxy S22 Ultra
- Samsung Galaxy S22 Plus
- Samsung Galaxy S22 5G
- Samsung Galaxy S22+ 5G
- Samsung Galaxy S22
- Samsung Galaxy S21 Ultra 5G
- Samsung Galaxy S21+
- Samsung Galaxy S21+ 5G
- Samsung Galaxy S21 5G
- Samsung Galaxy S21 Fan Edition 5G
- Samsung Galaxy S20 Ultra 5G
- Samsung Galaxy S20 Ultra
- Samsung Galaxy S20+ 5G
- Samsung Galaxy S20 5G
- Samsung Galaxy S20 FE 5G
- Samsung Galaxy S20 FE
- Samsung Galaxy S20+
- Samsung Galaxy S20
- Samsung Galaxy S10 5G
- Samsung Galaxy S10+
- Samsung Galaxy S10e
- Samsung Galaxy S10 Lite
- Samsung Galaxy S10
- Samsung Galaxy S9+
- Samsung Galaxy S9
- Samsung Galaxy S8+
- Samsung Galaxy S8 Active
- Samsung Galaxy S8
- Samsung Galaxy S7 Edge
- Samsung Galaxy S7 Active
- Samsung Galaxy S7
- Samsung Galaxy S Light Luxury

27 Samsung Galaxy A-Series smartphones:

- Samsung Galaxy A90 5G
- Samsung Galaxy A80
- Samsung Galaxy A73 5G
- Samsung Galaxy A72
- Samsung Galaxy A71 5G
- Samsung Galaxy A71
- Samsung Galaxy A70s
- Samsung Galaxy A70
- Samsung Galaxy A60
- Samsung Galaxy A52s 5G
- Samsung Galaxy A52 5G
- Samsung Galaxy A52
- Samsung Galaxy A51 5G
- Samsung Galaxy A42
- Samsung Galaxy A23 5G
- Samsung Galaxy A23
- Samsung Galaxy A20s
- Samsung Galaxy A11
- Samsung Galaxy A9 Pro
- Samsung Galaxy A9
- Samsung Galaxy A8 Star
- Samsung Galaxy A8s
- Samsung Galaxy A6+
- Samsung Galaxy A6s
- Samsung Galaxy A02s
- Samsung Galaxy A01

28 Samsung Galaxy M-Series smartphones:

- Samsung Galaxy M52 5G
- Samsung Galaxy M51
- Samsung Galaxy M42 5G
- Samsung Galaxy M40
- Samsung Galaxy M23
- Samsung Galaxy M11
- Samsung Galaxy M02s
- Samsung Galaxy M01

29 Samsung Galaxy J-Series smartphones:

- Samsung Galaxy J8
- Samsung Galaxy J7 V
- Samsung Galaxy J6+
- Samsung Galaxy J4+
- Samsung Galaxy J4 Core
- Samsung Galaxy J3
- Samsung Galaxy J2 Pro
- Samsung Galaxy J2 Core

30 Samsung Galaxy Note-Series smartphones:

- Samsung Galaxy Note20 Ultra 5G
- Samsung Galaxy Note20 Ultra
- Samsung Galaxy Note20 5G
- Samsung Galaxy Note20
- Samsung Galaxy Note10+ 5G
- Samsung Galaxy Note10+
- Samsung Galaxy Note10 5G
- Samsung Galaxy Note10
- Samsung Galaxy Note9
- Samsung Galaxy Note8
- Samsung Galaxy Note7

31 Samsung Galaxy F-Series smartphones:

- Samsung Galaxy F52 5G
- Samsung Galaxy F23
- Samsung Galaxy F02s

32 Samsung Galaxy Z-Series smartphones:

- Samsung Galaxy Z Flip5
- Samsung Galaxy Z Flip4
- Samsung Galaxy Z Flip3 5G
- Samsung Galaxy Z Flip 5G
- Samsung Galaxy Z Flip
- Samsung Galaxy Z Fold 4

- Samsung Galaxy Z Fold3 5G
- Samsung Galaxy Z Fold2 5G

33 Samsung Galaxy Fold/Folder-Series smartphones:
- Samsung Galaxy Fold 5G
- Samsung Galaxy Folder2
- Samsung Galaxy Fold

34 Other Samsung Galaxy smartphones:
- Samsung Galaxy C7
- Samsung Galaxy On7
- Samsung Galaxy Quantum 2
- Samsung Galaxy Xcover6

35 Samsung Galaxy Book Chromebooks and Laptops:
- Samsung Galaxy Book Go 5G
- Samsung Galaxy Book S LTE
- Samsung Galaxy Book Go

36 Samsung Galaxy Tab-Series Tablets:
- Samsung Galaxy Tab S9 Ultra
- Samsung Galaxy Tab S8 Ultra
- Samsung Galaxy Tab S8+
- Samsung Galaxy Tab S8
- Samsung Galaxy Tab S7 FE
- Samsung Galaxy Tab S7+
- Samsung Galaxy Tab S7
- Samsung Galaxy Tab S6 5G
- Samsung Galaxy Tab S6 Lite
- Samsung Galaxy Tab S6
- Samsung Galaxy Tab S5e
- Samsung Galaxy Tab S4 10.5
- Samsung Galaxy Tab S3 9.7
- Samsung Galaxy Tab S2 9.7
- Samsung Galaxy Tab S2 8.0
- Samsung Galaxy Tab A7 10.4
- Samsung Galaxy Tab A 8.0
- Samsung Galaxy Tab A 10.5
- Samsung Galaxy Tab Active4 Pro
- Samsung Galaxy Tab Active Pro

REQUESTS

37 The Claimant requests:

I. The Defendants are ordered,

1. to cease and desist, in the territories of the French Republic and/or the Federal Republic of Germany from

offering, placing on the market, using, importing or storing for these purposes an integrated circuit

comprising:

a plurality of functional blocks; and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the

functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data communication network comprising a first data router and a second data router interconnected through a first communication channel, characterized in that the first communication channel comprises M*N data storage elements, M being a positive integer, for delaying whole data packages including the routing information by introducing a delay of M*N cycles on the first communication channel,

(direct infringement of claim 1),

2. to cease and desist, in the territories of the French Republic and/or the Federal Republic of Germany from

   offering, placing on the market, using, importing or storing for those purposes a product obtained directly by a process including a method of designing an integrated circuit

   comprising:

   a plurality of functional blocks, and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface; characterized in that the method comprises:

   identifying a first communication channel between a first data router and a second data router that has a data transfer delay exceeding a predefined delay threshold; and inserting M*N data storage elements into the first communication channel, M being a positive integer, for delaying whole data packages including the routing information by introducing a delay of M*N cycles on the first communication channel

   (direct infringement of dependent claim 8),

3. with regard to the products referred to in section I.1. and I.2. which have been put on the market since 7 September 2011, at their own expense, to

   a. recall the aforesaid products from the channel of commerce by requesting in writing the respective commercial customers in possession of the

infringing products to return them to the Defendants, with reference to the fact that in the judgement to be designated the court addressed has found an infringement of the European Patent EP 1 875 683 B1, whereby the commercial customers are promised that in the event that the infringing products are returned, they will be refunded the purchase price already paid, if any, as well as the transport or shipping costs incurred as a result of the return, including any customs and storage costs,

b. definitely remove the aforesaid products from the channel of commerce by taking back the recalled products, and

c. hand over the aforesaid products in their direct or indirect possession or ownership to a bailiff to be appointed by the Plaintiff for destruction at the Defendants' expense or, at their option, to destroy the aforesaid products themselves or, at their option, to deprive the aforesaid products of its infringing property by removing and destroying the inbuilt infringing means;

4. to inform the Plaintiff of

a. the origin and distribution channels of the products referred to in section I.1. which have been put on the market since 7 October 2011,

b. the quantities produced, manufactured, delivered, received or ordered, as well as the price obtained for the products referred to in section I.1. which have been put on the market since 7 October 2011, and

c. the identity of any third person involved in the production or distribution of the products referred to in section I.1. which have been put on the market since 7 October 2011;

5. to pay to Plaintiff an interim award of damages in an amount at the discretion of the Court.

II. Each individual failure to comply with any order pursuant to sections I.1. to I.5. will render the respective Defendant liable to pay to the Court a possibly repeated penalty of up to EUR 250,000.00 per day for each day the respective Defendant fails to comply.

III. The Defendants are liable for all damages resulting from the patent infringement as specified under section I.1. since 7 October 2011 in the territories of the French Republic, the Federal Republic of Germany and the United Kingdom of Great Britain and Northern Ireland.

IV. The Plaintiff is permitted, at Defendants’ expense, to display the decision and publish it in full or in part in a daily newspaper with nationwide circulation in each of the territories referred to in section I.1. and I.2.

V. The Defendants are to bear the legal costs jointly and severally.

VI. The aforesaid orders are immediately enforceable. In the event that a security is ordered, the Plaintiff is permitted to provide security by bank or savings bank guarantee. The amount of the security shall be determined separately for each enforceable order. The Claimant considers the following partial security to be appropriate:

Section I.1., I.2. (cease and desist): 70 % of the total security

Section I.3.a, I.3.b (recall and removal): 10 % of the total security

Section I.3.c (destruction): 5 % of the total security

Section I.4 (information): 7,5 % of the total security

Section I.5 (interim damages): 5 % of the total security

Section IV (notice of judgment): 2.5 % of the total security.

38 The Defendants request:

I. The complaint is rejected.

II. Claimant is ordered to pay the costs of the proceedings.

III. Claimant is ordered to provisionally reimburse the costs of Defendants 3) to 5).

Alternatively:

IV. The enforcement of the decision is subject to an appropriate security to be determined by the Court and to be provided by Claimant.

V. The decision, including the orders contained therein, is made subject to the condition precedent that the patent-in-suit is not held to be wholly or partially invalid by the final decision – alternatively a first instance decision – in (other) revocation actions, including counterclaims for revocation.

Auxiliary:

The decision, including the orders contained therein, is made subject to the condition subsequent that the patent-in-suit is held to be wholly or partially invalid by the first instance decision – alternatively the final decision – in (other) revocation actions, including counterclaims for revocation.

39 The Claimant requests,

to reject Defendants' 3), 4) and 5) requests under III., IV. and V.

40 For the Counterclaim for revocation, the Defendants request:

I. European Patent 1 875 683 B1 is revoked in its entirety for the territory of Germany and France.

II. Claimant is ordered to pay the costs of the proceedings regarding the Counterclaim for revocation.

III. Claimant is ordered to provisionally reimburse the costs of Defendants 3) to 5).

41 The Claimant requests in the Counterclaim for revocation:

I. The Counterclaims for revocation of the Defendants 3), 4) and 5) are rejected.

II. Defendants 3), 4) and 5)'s request that the Claimant is ordered to provisionally reimburse the costs of the Defendant is rejected.

III. Defendants 3), 4) and 5) are ordered to jointly pay the costs of the proceedings regarding the counterclaims for revocation.

POINTS AT ISSUE

Standing to sue

42 The Claimant considers himself to have standing to sue. Claimant and Philips are in agreement that the patent-in-suit and its annex claims have been transferred effectively. A third party as the Defendants cannot challenge that. Against this background, the Claimant has standing to sue unless the Defendants can prove otherwise by substantially disputing facts which they did not. Furthermore, the entry in the respective patent register provides the (refutable) assumption that the registered individual/company is the actual proprietor, which is the case here. This cannot be eliminated by simply disputing. Finally, as a mere precaution, the Claimant relies on the PPA and PAs submitted as Exhibits P 24 and P 25, which, according to the Claimant, show that the patent-in-suit and all claims have been effectively transferred. The Claimant particularly states that the signatories of the agreements were duly authorised as confirmed by several witness statements.

43 The Defendants are of the opinion that the Claimant does not have standing to sue for the asserted claims. The Claimant has neither shown that it has validly acquired the patent-in-suit, nor that the claims for the past have been validly assigned to the Claimant. In clear contradiction to the front-loaded system, the Claimant did not provide any evidence in its Statement of claim of an effective assignment of claims for the period before the (alleged) acquisition of the patent-in-suit, nor did the Claimant provide any evidence for the effectiveness of the alleged transfer of the patent-in-suit. The burden of proof for the effective patent assignment lies with the Claimant.

44 Insofar as the Claimant has submitted a PPA and corresponding PA, the Defendants argue that these documents have been late-filed and must not be considered. Notwithstanding this, the Defendants dispute, based on different colours and formats of single pages of the PPA, which are also partly tilted, that Exhibit P 24 is a true copy of the original PPA (ink version), as signed by the parties to the PPA, including the exhibits thereto, in particular Exhibit A to the PPA. They also dispute that the patent-in-suit is listed in the original PPA (ink version), as signed by the parties to the PPA.

45 The Defendants further dispute that the conditions in sec. 4.1 PPA were fulfilled, in particular that the purchase price was received by Philips in full at the Closing and that the assignment of the patent-in-suit was unhindered by the Encumbrances, Identified Agreements and Current Agreements. The Defendants dispute that sec. 4.1 PPA covers the asserted claims and they dispute, in particular, that it was Claimant's and Philips' intention to assign such claims with the PPA. The Defendants further dispute that the asserted claims under the patent-in-suit were validly acquired by the Claimant by means of the PAs. They dispute that it was Claimant's and Philips' intention to assign the patent-in-suit with the PAs (anew) and that the PAs were correct in the sense that the assignment happened by means of the PPA before. Finally, the Defendants dispute that the signatories to the PPA and the PA had the authority to sign.

Claim construction

46 Regarding claim 1, the Claimant is of the opinion that the term "integrated circuit" (IC) is used in the patent-in-suit under its normal meaning in the art, i.e. meaning a circuitry on a chip. An IC is an assembly of electric components such as transistors, resistors and capacitors, interconnected on a semiconductor material. The skilled person would understand that Systems on Chip (SoC) are also ICs according to patent-in-suit. The functional block mentioned in claim 1 may be, for example, a processing unit. Insofar as a data communication network is required, this network relates to a network on chip (NoC). It is a so-called packet-based network as data packages are communicated between the functional blocks in accordance with the technical teaching of claim 1.

47 According to the Claimant, the N data elements of a data package refer to a size of the data package. The term "data package" is defined as comprising N data elements at least one of which comprises routing information for the network stations. Under "routing information", the skilled person would understand information relating to the routing of the data package through the network. For example, this routing information may include information on the destination

and required service of the data package. The Claimant specifies that the terms “data package” and “data packet” do not necessarily denote the same grouping of data elements, and that a data package is nothing more (nor anything less) than a grouping of at least two data elements. With regard to the M*N data storage elements, the person skilled in the art would realise that the size of a data package needs to be fixed (i.e. contain N data elements), but only in relation to the particular hardware element containing the M*N data storage elements, i.e. in relation to the number of data storage elements.

48 The Claimant further explains that the communication channels within the meaning of the patent-in-suit may, for example, comprise one or more wires, such as data buses and serve the transmission of data. Under “data router”, the skilled person would understand a networking device that routes data (in particular, data packages) across the network (based on routing information included in data packages) so that the data arrives at their destination. The patent-in-suit is not limited to any particular routing technique and describes both wormhole routing and store and forward routing as examples. The network interfaces are interfaces between the data routers and the functional blocks. Among the routers and communication channels, claim 1 identifies a first and a second data router interconnected through a first communication channel. The Claimant points out that this can be any communication channel and data routers interconnected thereby. As example, the patent-in-suit describes the first communication channel may be the slowest channel of the network exhibiting a data transfer delay exceeding a predetermined delay threshold.

49 The Claimant finally refers to the requirement of the invention that the first communication channel comprises M times N data storage elements. It is of the opinion that a data storage element may, for example, be a pipeline or a buffer of latches or flipflops and may be implemented using synchronous or asynchronous storage elements. The number of storage elements is a multiple of N, i.e., a multiple of the size of a data package whereby M can equal 1. As the data storage elements introduce a delay on the first communication channel of M times N cycles, whole data packages, including the routing information, will be delayed, rather than a single data element. The Claimant points out, that, as a result, the correct periodicity between the network stations can be maintained, upon which the correct operation of the network relies. However, according to the Claimant, it is not a purpose of the M*N data storage elements that the arrival of the whole data packages occurs at the recipient at a time when the recipient is ready to process the routing information.

50 Claim 8 relates to a method of designing an integrated circuit that corresponds to an integrated circuit according to claim 1. Claimant states that claim 8 differs from claim 1 only in that the first communication channel has a data transfer delay exceeding a predefined delay threshold.

51 The Defendants point out with regard to claim 1 that the patent-in-suit does not contain a definition of the term integrated circuit. Usually, an integrated circuit means a chip, i.e. a multiplicity of components, such as transistors, resistors, and capacitors, arranged and interconnected on a substrate of semiconductor material. The IC according to the patent comprises a plurality of functional blocks which are regarded to be any kind of processing unit.

The data communication network required by the technical teaching of claim 1 and 8 is part of the integrated circuit, i.e. a network-on-chip. The term “network stations” used in the claims is further defined and includes routers and network interfaces. The network stations are interconnected via communication channels which may be understood as path segments the data travels along the network such as between two routers. As the data is transmitted in data packages, the claims relate to a packet-based network. According to the Defendants, a “router” within the meaning of the patent-in-suit is a networking device that routes data (in particular, data packages) across the network (based on routing information included in the data packages) so that the data arrive at their destination. A “network interface” is defined to be the component that provides the conversion of the packet-based communication of the network to the higher-level protocol that the higher-level modules, i.e. the functional blocks, use. While the network stations are interconnected via communication channels, one connection between a first router and a second router is termed first communication channel. According to the patent-in-suit, this first communication channel may be the one with a data transfer delay exceeding a predetermined threshold. Claim 1 does not contain such a requirement, whereas claim 8 requires that the first communication channel is the slowest one.

52 The Defendants are of the opinion that, according to claim 1, every data packet communicated within the NoC by the network stations has a fixed size of N data elements with N being an integer of at least two, wherein one of these data elements comprises routing information. “N” cannot vary from data package to data package. This is not only clear from the language of claim 1 (“each data package”) but also from the interplay with the requirement of M*N data storage elements in the first communication channel. The number of data elements (N) corresponds to the number of data storage elements (see below) and thus to the delay of data which in turn depends on the communication channels in the hardware. Since the network and the communication channels are configured prior to use, N is an integer set at the time of designing the NoC and fixed for the lifetime of the NoC. The Defendants point out that this understanding is shared by the Patent Trial and Appeal Board (PTAB) of the United States Patent and Trademark Office (USPTO) and confirmed by the Claimant in Inter Partes Review (IPR) proceedings (IPR2024-00355) against US 8,072,893, the US counterpart to the patent-in-suit.

53 The Defendants argue that, according to the patent specification, the invention is based on the realisation that the correct operation of the network depends on maintaining the correct periodicity, which is related to the fixed size of the data package. If the size were variable, a delay which matches the period of N cycles would be impossible. Rather, the constant (or fixed) number of data elements of the data packages communicated via the communication channels directly determines whether the “correct periodicity” and the “appropriate period” can be maintained in the NoC. Accordingly, the routers are all configured to periodically evaluate the content of a received data package at the same clock cycle after every N clock cycles for data packages having N data elements. This is due to the fact that all data packages have a fixed size of N data elements, with the consequence that the communication of a complete package between two network stations takes N clock cycles. Further, the routing information has a fixed position in the header of a data package. The introduction of a delay on the slowest

communication channel requires a delay of the entire data package, i.e. N clock cycles so that the data package can be received at the target network station during the expected clock cycle. In the event of a deviation, the network would not maintain the correct periodicity between the network stations and would lose its deterministic behaviour. The preferred embodiments of the patent specification correspond to this understanding.

54 The Defendants explain that, for delaying whole data packages, claim 1 further requires that the number of data storage elements inserted into the first communication channel is related to the number of data elements N of each single data package. The "correct periodicity" is not altered when inserting multiples of N storage elements into the first communication channel. The purpose of the claim is thus that the data package's transmission over a communication channel is delayed such that the arrival of the "whole data packages including the routing information" at the recipient occurs at a time when the recipient is ready to process the routing information. The Defendants argue that the arrival of the routing information at the right time, and thus the delay according to the "M*N" specification, is not a preferred option of the teaching of the patent-in-suit. Rather, any mismatch of storage elements and size leads to the claimed solution no longer working. That is why the Defendants refute Claimant's opinion that a purpose-related limitation should not be read into the claim. If only some data packages had N data elements, data packages with more or less than N data elements could not be delayed and the periodicity of their arrival could not be ensured. The Claimant argues that, only if "data packages" are understood to be "data packets" in the meaning in the art, consisting of a fixed number of data elements, whereby the number is mathematically strictly related to the number of the data storage elements, will the transmission over the communication channel be successful and the routing information be received during the appropriate period. This is exactly what the former proprietor of the patent-in-suit explained to the examiner when delimiting the technical teaching of the patent over a prior art document (BP-CR 4). The meaning of the term "data package" comprising "N data elements" is also confirmed if the statements in the context of the claim amendments during Examination before the European Patent Office are taken into account. Claim 1 further requires that the storage elements are comprised by the first communication channel which refers to a physical circuitry, including wires and storage elements.

55 Unlike claim 1, claim 8 additionally requires that the first communication channel is the slowest.

Validity

56 The Defendants are of the opinion that the subject matter of claims 1 and 8 are inadmissibly extended beyond the content of the patent application. They believe that the claim language constitutes an inadmissible intermediate generalization of what is described in the application as originally filed since the patent application describes not only that a whole data package is delayed but also that a complete data package is transmitted within the N clock cycles onto the communication channel. The latter was however not included in the claim language when the claim was amended during the examination phase and the feature "delaying whole data packages including the routing information" was added.

57 The Defendants are also of the opinion that claims 1 and 8 of the patent-in-suit including the dependent claims lack novelty over Bertozzi et al., “Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-Chip”, published on 3 September 2004 in IEEE Circuits and Systems Magazine (Vol. 4, Issue 2, 2004) (submitted as Exhibit BP-CR 1). In particular, BP-CR 1 discloses data packages in the form of “fixed length packets” which in turn are subdivided into flow control units, so-called “flits” which require one clock cycle for transmission and can be regarded as data packets within the meaning of the patent-in-suit. Figure 3 of BP-CR 1 depicts the packet partitioning into ten flits which also comprise the routing information of the packet. The Defendants argue that BP-CR 1 also discloses a first communication channel of the network comprising M*N data storage elements for delaying whole data packages for M*N clock cycles according to the invention. In this respect, Defendants essentially refer to explanations in BP-CR 1 according to which link throughput can be decoupled from the length of the wire by inserting pipeline stages. They are of the opinion that figure 4 of BP-CR 1 discloses a link between two switches comprising four data storage elements in the form of four repeater stations and four flits of one data packet. This would disclose the teaching of the patent in suit.

58 In case the Court has doubts on a disclosure of the delaying of whole data packages by M*N data storage elements, the Defendants argue that the invention of the patent-in-suit is at least obvious to the skilled person when BP-CR 1 is considered in combination with US patent 6,081,844 (Exhibit BP-CR 2) or with S. Hassoun et al., “Optimal Buffered Routing Path Constructions for Single and Multiple Clock Domain Systems”, ICCAD 2002 (Exhibit BP-CR 3). When aiming at an improvement of the data transfer within a NoC, the skilled person would have looked at the pre-existing networks and communication path constructions disclosed in BP-CR 2 and 3 since the problem of delayed packets due to the link length is well known in the art and is also addressed in BP-CR 2 and 3. Therefore the skilled person would arrive at the subject matter of claim 1 without exercising inventive skill.

59 An alternative starting point in the Defendants’ view is Dielissen et al., “Concepts and implementation of the Philips Network-on-chip”, IP-Based SoC Design 2003; S. 1-6, published on 13 November 2003 (Exhibit BP-CR 4). Even if BP-CR 4 does not describe a first communication channel comprising M*N data storage elements for delaying whole data packages by introducing a delay of M*N clock cycles, the combination with BP-CR 2 or 3 renders the invention under the patent-in-suit obvious.

60 The Claimant argues that the addition of the feature “Delaying the whole data package” is merely a clarification of a feature that was already present in originally filed claim 1. The original claim 1 already contained the feature that a delay of M*N cycles is introduced. This feature means that the whole data package is delayed rather than a single data element.

61 The Claimant is of the opinion that BP-CR 1 does not disclose a communication channel comprising M*N data storage elements, the number of which correlates with the N data elements of a data packet. Therefore, a delay of a whole data package by introducing a delay of M*N clock cycles is also not revealed. Figure 4 of BP-CR 1 does not address the structure

of data packets and the number of flits contained in such packets. Instead, Figure 3 of BP-CR 1 confirms that a packet comprises 10 flits. BP-CR 1 simply does not suggest any correlation between the number of repeater stages and the number of flits depicted in Figure 4. Furthermore, the Claimant argues, that BP-CR 1 does not disclose that the number of repeater stages in a link is a function of (or correlates with) the number of flits. Instead, the skilled person would understand that the number of repeater stages is a function of (or correlates with) a desired length of each segment. BP-CR 1 even discloses that the switches must be latency-insensitive in order to correctly operate regardless of the number of repeater stages on a link. This allows an arbitrary number of repeater stages.

62 The Claimant further argues that, for the aforementioned reasons, BP-CR 1 cannot be a promising starting point for the skilled person in order to arrive at the technical teaching of the patent-in-suit. Rather, BP-CR 1 teaches away from the claimed invention. Irrespective of this, BP-CR 2 and 3 do not disclose M*N data storage elements which are arranged in a first communication channel of a Network on Chip and correlated with the number of data elements per data package for delaying whole data packages. Therefore, the technical teaching of the patent-in-suit is not obvious.

Attacked embodiment

63 The Claimant considers the “infringing embodiments II and IV” as the attacked embodiments in general and not limited to specific models. All products which incorporate, implement, utilise, include, or otherwise comprise NoCs designed using tools from the company Arteris Inc. (“Arteris NoC”) or NoCs which are materially similar (core-identical) to such Arteris NoCs are attacked. The Claimant argues that it is sufficient to demonstrate that a sample of the attacked embodiment, here: the Snapdragon 8+ Gen. 1, realises all features of the asserted claims. For all other attacked embodiments, it is sufficient to state that they are ‘core-identical’ or ‘materially similar’ as the Claimant did. As long as the Defendants do not argue differently, they must be considered as infringing.

64 The Defendants consider only the processor Snapdragon 8+ Gen. 1 as attacked embodiment because the Claimant merely bases its infringement allegation on this single IC model. They argue that the Claimant, instead of identifying only this model and relying on similar models being included, has chosen to explicitly name a large number of models that are also said to be attacked. But then the Claimant must also show that all of these models use the patent-in-suit, because all of these are at issue. Otherwise, Defendants would be burdened with reviewing all of the named products and reply accordingly, which would be inappropriate. The Claimant has however not provided any reasons as to why the other 200+ listed “infringing embodiments II” should be “core-identical” or “materially similar” to that model with regard to the patent-in-suit. Insofar, the Claimant’s statements are inconclusive. At least one example, the processor MSM6000 uses fundamentally different technology than the Snapdragon 8+ Gen. 1 as it has no NoC and has already been on the market since 2002. Beyond the MSM6000, there are further models listed which were already publicly available before the priority date of the patent-in-suit without using any NoC technology.

Infringement

65 The Claimant takes the view that the infringing embodiments II and IV realise the technical teaching of claims 1 and 8. It states that Qualcomm NoC ICs are integrated circuits comprising at least two functional blocks, for example a central processing unit, a graphics processing unit and/or a secure processing unit.

66 The Claimant asserts that the infringing embodiment II – the Qualcomm NoC ICs – comprise a data communication network in form of the Arteris NoC designed according to the Arteris NoC Chapter. This could be inferred from the fact that the Defendants, according to the press releases and Arteris' statements on its website, use Arteris NoC IP technology for over a decade at least in their Snapdragon application processors, LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products and even acquired Arteris NoC technology including Arteris employees in 2013. In the Claimant's view, this shows that the Defendants rely on Arteris NoC technology in their ICs. Irrespective of this and even if the infringing embodiment II does not implement the Danube NoC IP blocks library and the Qualcomm NoC design tool does not make use of the NTTP packet structure, it can be inferred from the Defendants' submissions that the infringing embodiment II realises the teaching of claim 1 of the patent-in-suit.

67 The Claimant explains that the Arteris NoC comprises routers and network interface units, hence network stations within the meaning of the technical teaching of the patent-in-suit. The network interface units (NIUs) are also interfaces between functional blocks and data routers, which are thus coupled to a functional block. The network stations are interconnected via communication channels which are communicating data packages between the functional blocks because the Arteris NTTP protocol is packet-based. Packets are created by the NIUs and transported to other parts of the NoC. According to the Claimant referring to the Arteris NoC Chapter, the packets are comprised of cells such as a header cell, an optional necker cell and possibly one or more data cells. The Claimant argues that the cells are data elements in the sense of the patent-in-suit and, thus, the packets of the Arteris NoC have a size of at least two data elements. The header and necker cells also contain the required routing information.

68 The Claimant disputes the Defendants' argument that each "data packet" must have a fixed size and the patent-in-suit is not infringed as [redacted]. In the Claimant's view, claim 1 is not limited to a "fixed packet size". The "data packets" mentioned by the Defendants do not necessarily denote the same grouping of data elements of a "data package". The "Data package" is what is grouped in N data elements whereby N depends on the data storage elements contained in the communication channel.

69 The Claimant is of the opinion that the Arteris NoC comprises a first communication channel interconnecting a first and second data router. This channel comprises M*N data storage elements for delaying whole data packages by introducing a delay of M*N cycles on the channel. The Claimant refers to

- delay pipelines which are described in the Arteris NoC Chapter and are automatically inserted to keep data and routing information in phase. In the Claimant's view, such delay pipelines correspond to data storage elements in the sense of the patent-in-suit and, as they keep data and routing information in phase, will cause a delay of whole data packages which corresponds to M times N data storage elements.
- muxes, synchronous FIFOs, and width and endian converters as further units for routing and transmitting data over long distances.
- input pipes of the Arteris NoC which introduce FIFOs. FIFOs are buffers and correspond to data storage elements in the sense of the patent-in-suit. They introduce a delay of M times N cycles when accomplishing "timing closure."
- a parameter called "fwdPipe" introducing pipeline registers, and pipelining in different NoC element instances, which are other examples for storage elements delaying data packets are.

The Claimant argues that all these data storage elements mentioned before are included in a communication channel in order to "close timing", so that the periodicity of the network stations is maintained, and to convert data elements with different properties and characteristics. Timing closure and adaptation for different properties and characteristics are both accomplished by introducing a delay of M times N cycles.

70 In particular, the FIFOs and width converters are inserted in the links, i.e. the communication channels, according to the Arteris NoC Chapter. The Claimant argues that these pipelining components are indeed data storage elements, which delay whole data packages including routing information by introducing a delay of M*N cycles. Width converters adapt different link widths. To this end, a FIFO buffer is implemented in the design phase of the NoC, which, for example, as a so-called 4-to-1 converter stores 4 data elements, each of 8 bit chunks, so as to be able to output 32-bit wide data. In the example, the width converter has 1*4 data storage elements for delaying whole data packages, thereby introducing a delay of 1*4 (M*N) cycles on the link. The data package is formed by the data elements stored in the width converter. Its size corresponds to the buffering space, which is N = 4 in the example.

71 Another example of "data storage elements" are "rate adapters" implemented in the links between the endpoints of the Noc according to the Arteris NoC Chapter. They delay whole data packages in a similar way as the width converters, although they adapt the rate instead of the data width.

72 The Claimant points out that when the Defendants dispute the use of M*N data storage elements, they refer only to „pipeline stages" and not to any of the other "data storage elements." However, there is additional evidence that the infringing embodiments are indeed implementing M*N data storage elements. In this regard, the Claimant argues that the infringing embodiments have support in Linux whose kernel contains drivers for Qualcomm products. Within the drivers, there is a subsection for interconnects and in that subsection several companies, including Qualcomm, have code for their products. The Linux 6.0.1 Kernel is publicly available and shows that Quality of Service ("QoS") was a configurable feature spanning Qualcomm products from 2013 through at least 2021. The QoS configuration

includes configurable control parameters including priority for a specific node with the NoC interconnect of Qualcomm products (see file “icc-rpm.h”, Exhibit 18). The source code shows that Qualcomm ICs include ports having different bus widths (for example, file “sm8450.c”, Exhibit 18). Consequently, converters in terms of width and/or rate will be implemented. As prioritisation is applied as part of QoS, data packages will be prioritised over these different bus widths, which implies that one must be able to buffer (non-prioritised) data packages and that conversion will be happening in the network nodes that are QoS controlled. The Claimant assumes that, in turn, storage elements, such as those embodied in the form of width converters or rate adapters, will be used that cause a delay in accordance with the claimed technical teaching.

73 The Claimant is of the opinion that the requirement of introducing a delay of M*N cycles by M*N data storage elements within the first communication channel is literally realised. However, if the court ruled that the data storage elements are not in the communication channel, but at least partly in the routers or other components of the Arteris NoC, the Qualcomm NoC ICs infringe the patent-in-suit by equivalence.

74 The Defendants are of the opinion that the Arteris NoC Chapter (Exhibit P 10) does not show a realisation of the teaching of claim 1 of the patent-in-suit.

75 The Defendants point out that the Arteris NoC Chapter only describes that “*All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells.*” They take the view that not all packets comprise the same N data elements as the only constant element is the “header” and the remaining elements are optional. The reference to “one or more” data cells shows that even the amount of data elements is variable. Thus, the data packages transmitted in accordance with the Arteris NoC Chapter are of variable size.

76 The Defendants further argue that none of the various measures – optional or mandatory – mentioned in the Arteris NoC chapter and referred to by the Claimant to support its allegation of a delay of whole data packages by M*N cycles demonstrate the realisation of the teaching of the patent in suit.

77 The Defendants point out that
- the delay pipelines according to the Arteris NoC Chapter are part of the input controller, hence of the router, not of the communication channel. The patent-in-suit differentiates between storage elements arranged inside a switch/router and inside the communication channel. Claims 1 and 8 are limited to the latter.
- the pipelining components mentioned by the Claimant are not used for delay purposes but for a different reason, which is directly derivable from the Arteris NoC Chapter. They do not delay data packages by M*N cycles.
- the input pipes are one-word-deep FIFOs arranged inside the router/switch. A “word” within the meaning of the Arteris NoC Chapter is similar to a cell, i.e. a data element according to the Claimant.

- the parameter “fwdPipe” depends on the designer including pipeline registers. However, the designer is not obliged to exactly choose a specific number of pipelining registers, or that these are in any way connected to the number of data elements of data packets.
- even if it were true that automatically inserted pipelines (Exhibit P 13) are data storage elements inserted to achieve a specific periodicity, this would give no hint that exactly M*N data storage elements are used. If long wires are only divided into shorter pipeline stages, this does not differ from prior art.
- slide 4 of Exhibit P 12 does not differ from prior art and only adds a number of pipeline stages according to the (physical) length of the wire.
- general pipelining data storage elements appear to be a summary of all the measures previously mentioned by the Claimant.

78 With regard to FIFOs mentioned in the Arteris NoC Chapter and referred to by the Claimant, the Defendants argue that, according to this section of the Arteris NoC Chapter, FIFOs delay data for avoiding congestion, but nothing points towards a certain number, namely, M*N FIFOs. In any event the number of FIFOs introduced into communication channels of the attacked embodiment, is not dependent upon the number of data elements.

79 Irrespective of this, the Defendants even dispute that Qualcomm NoC products, i.e. the infringing embodiments II and IV, were designed identical to “Arteris NoCs” described in Chapter 11 of the book “Networks-on-Chips Theory and Practice”, submitted as Exhibit P 10. The Arteris NoC Chapter does not describe NoCs on Qualcomm chips. It is rather directed to proprietary Arteris technology which differs from the design used for Qualcomm NoCs. The Defendants are of the opinion that the press releases relating to Arteris NoC technology used in the Defendants’ processor applications and to the acquisition of Arteris technology by Qualcomm in 2013 do not support Claimant’s allegation that any NoCs in Qualcomm chips are identical to any Arteris NoC’s. This allegation is factually incorrect. According to the Arteris NoC chapter, Arteris proposes a complete commercial solution for SoC communication architecture, which is based on the Danube NoC IP block library. However, the Qualcomm’s design tool does not comprise the Danube NoC IP block library.

80 The Defendants state that the Qualcomm NoC products do actually not implement the technical teaching of the patent-in-suit. [redacted].

81 The Defendants explain that the attacked embodiment transmits “data packets.” They argue that a data package of a certain size cannot be arbitrarily selected but has to be related to the data packet transmitted in the attacked embodiment. The Defendants state that each “data packet” consists of one or more words. A word is a fixed-size group of bits equal to the size of the data bus the word is being transmitted on. [redacted], i.e. they do not contain the same number of words. Thus, [redacted]

[redacted], the routing information does not arrive at the network interfaces or routers/switches at any defined, consistent interval.

82 [redacted].

83 As to the Linux drivers, the Defendants argue that the Claimant fails to show any specific use of the software files in connection with width converters or rate adapters, much less how the software shall provide a hint towards the M*N requirement of the patent-in-suit. The Claimant only formulates a hypothesis that there must be width converters and/or rate adapters implemented, due to the fact that different bus widths are present. However, the Claimant fails to substantiate this allegation by either showing the actual hardware components or pointing to sections of the code which may show how such an alleged width converter and/or rate adapter shall functions.

84 With regard to width converters, the Defendants take the point of view, that such a converter is not at all a tool for maintaining the correct periodicity between the network stations. They only connect a signal path of one width to a signal path of a different width. As they link two signal paths, it is already questionable how they can be arranged in a communication channel. The Defendants additionally argue that the width converters mentioned by the Claimant are not used in the attacked embodiment to delay whole data packets by a specific number of cycles. Although some width converters may contain registers to store data words, the number of registers is not related to the size of the data packets [redacted]. The Defendants dispute that the example of a 4-to-1 converter made up by the Claimant has anything to do with the Qualcomm NoC products. They point out that this example must have four storage elements. [redacted]

[redacted].

85 According to the Defendants, the same applies to rate adapters [redacted]. Again, the Claimant uses the hypothesis that due to the fact that different bus widths are used, rate adapters would need to be used. However, the Claimant fails to show what specific element of the Qualcomm NoC it is referred to. Furthermore, the Defendants dispute that [redacted]. If any delay is created by a particular rate adapter, it varies depending on several factors and will not be the same for every data packet in the NoC.

86 Insofar as Claimant alleges that in case the Court requires the storage elements to be inserted into the communication channel the patent-in-suit is infringed by equivalence, Defendants are of the opinion that the Claimant has not named any substitute means for any type of the attacked embodiment and that it would not be appropriate if the Claimant's equivalent infringement theory was successful as it dissolves the specific teaching of the patent-in-suit.

Infringing acts

87 The Claimant argues that Defendants 3) and 4) offer, distribute, import and store the attacked embodiment, inter alia, in Germany and France. Defendant 3) is responsible for the website "www.qualcomm.com" and advertises the attacked embodiment there. Additionally, Defendant 3) provides a "Sales Support" and a list of distributors on its website, where the infringing embodiments can be purchased. These partners are verified to offer, sell and recommend products by Defendant 3) and Defendant 4). Defendant 4) is listed on the footer of the website www.qualcomm.com/ and its subdomains as follows: "Snapdragon and Qualcomm branded products are products of Qualcomm Technologies, Inc. and/or its subsidiaries." The Claimant therefore takes the view that Defendant 4) is offering the infringing products on the Website because without the consent no offering would be possible.

88 The Claimant further states that Defendant 4) sells products including the attacked embodiments to manufacturers that use, amongst other products the attacked embodiments, to include them in a broad range of devices, including but not limited to mobile devices, wireless networks etc. On their website an overview of Defendants' 3) and 4) business partners is provided. The list includes German and French partners, but also international partners, manufacturing mobile devices which are sold in Germany and France. The Defendants 3) and 4) know or even actively support that products in which their infringing

embodiments are built in are distributed in Germany and France. In particular, Defendants 3) and 4) distribute their infringing ICs to Samsung Electronics Co., Ltd., the former Defendant 1), for implementation and use in its electronic devices. Furthermore, Defendant 3) and Defendant 4) import and store their ICs – which are also predominantly manufactured in Asia – throughout Europe and especially in Germany and France, in particular for the purpose of distribution.

89 The Claimant further asserts that Defendant 5) markets, sells and distributes products of Defendant 3) and Defendant 4) in Europe, especially in Germany and France. It infers this from Defendant's 5) entry in the German company register. According to the Claimant, it is at least undisputed that Defendant 5) offers the infringing embodiments in France and in Germany. As far as the Defendants dispute that the Defendant 5) has placed the infringing embodiment on the market or imported or stored the same in Germany and/or France during the lifetime of the patent-in-suit, it is sufficient to help someone to place the attacked embodiments on the market. This is exactly what Defendant 5) did.

90 The Defendants state that no Samsung devices containing Qualcomm ICs were/are offered, placed on the market, imported and/or stored in Germany and/or France by the Defendants 3) and 4). Rather Samsung did/does so – and appears now, after the settlement with the Claimant, to be entitled to do so. Moreover, neither Defendant 3) nor Defendant 4) has itself placed on the market, imported and/or stored any Qualcomm NoC products in Germany and/or France during the lifetime of the patent-in-suit. Nor did the Claimant present the requirements of a "wilful collaboration" for the alleged attribution of infringing acts. In the Defendants' view, referring to "collaborators" shown on the website www.qualcomm.com/products/automotive/partners is not sufficient, taking also into account that there is no relation to the Qualcomm NoC products. The Defendants are of the opinion that the mere position of Defendant 3) as a parent company of the Qualcomm group cannot establish their liability as such, as this would lead to a strict liability of the top level entity. Even if one assumes that Defendants 3) and 4) know that at least some of the Qualcomm NoC products finally found their way on the market in Germany and/or France, this knowledge alone cannot establish a liability of the, themselves non-selling Defendants 3) and 4).

91 Insofar as the Claimant has stated that the Defendants 3) and 4) distribute their ICs to the former Defendant 1) for implementation and use in its electronic devices, the Defendants are of the opinion that these acts of distribution cannot constitute infringing actions in Germany and/or France since the Defendant 1) is located in the Republic of Korea. With regard to the alleged "offering" of the Snapdragon 8+ Gen. 1, the Defendants consider the Claimant's statements to be inconclusive.

92 The Defendants state that the Defendant 5) did not place any Snapdragon 8+ Gen. 1 on the market in Germany and/or France, nor did it import and/or store any Snapdragon 8+ Gen. 1 into/in Germany and/or France during the lifetime of the patent-in-suit. Beyond that, the Claimant merely refers to the excerpt from the German company register which does not reflect what Defendant 5) actually does and did over time.

Exhaustion

93 The Defendants further invoke the principles of exhaustion and therefore request that the Claimant and third parties (Samsung, Arteris) be ordered to produce several patent license agreements. The Defendants are of the opinion that the claims asserted by Claimant are unfounded to the extent that products are concerned, which fall under the scope of the license agreements in place between Claimant and RPX Corporation coming into effect as of 31 May 2024 ("RPX Agreement") on the one hand and between RPX and Samsung and RPX and Arteris on the other. The Claimant's rights must be exhausted with regard to the allegedly infringing products (i) manufactured and supplied by Samsung to Qualcomm and/or (ii) using "tools" and/or "NoC technology" from Arteris, if such use should form the basis for assuming infringement of the patent-in-suit. Insofar as Claimant argues that chips manufactured by Samsung and supplied to Qualcomm were excluded from the license, it must be taken into account that exhaustion is a legal effect provided for by law which cannot be circumvented by contractual agreements. Hence, the Claimant itself has shown that any chips supplied by Samsung to Qualcomm are licensed and, insofar, the principle of exhaustion applies. Even if "Arteris was merely granted a covenant to sue last", exhaustion is not excluded as the consent of the patentee to distribute the product does not necessarily have to be in the form of a license.

94 The Defendants further argue that the claims asserted by the Claimant are also inadmissible or at least unfounded, to the extent that the Qualcomm NoC products supplied by the Defendants were used in vehicles of the Volkswagen group. This objection is based on the Covenant not to sue included in the settlement agreement(s) between Claimant and Volkswagen AG and Audi AG and is raised as a defense by Defendants with regard to all Qualcomm NoC products supplied directly or indirectly by any of the Defendants.

95 The Claimant believes that the Defendants cannot successfully rely on an exhaustion defence. The RPX Agreement explicitly excludes the chips manufactured by Samsung and supplied to Qualcomm from the license granted to Samsung (via RPX). Additionally, also Arteris did not get a license from the Claimant.

Statutory limitation of claims

96 The Defendants are further of the opinion that the claims asserted by the Claimant in the Statement of claim are partially time-barred. For each individual claim, they explain why and to what extent they believe it is time-barred under the respective national German or French law. In particular, they argue that Philips must have known already way before 2020 that the attacked embodiment makes use of the patent-in-suit, if following the infringement mapping of Claimant.

97 The Claimant argues that national statute of limitations does not apply to the claims asserted, but rather Art. 72 UPCA the requirements of which, however, are not met.

Proportionality

98 Finally, the Defendants take the view that the requests must at least be rejected for lack of proportionality, which the Claimant contests.

GROUNDS FOR THE DECISION

99 Both the Counterclaim for revocation and the Infringement action are admissible, but unfounded.

Part 1: Admissibility

100 The Counterclaim for revocation and the Infringement action are admissible

A Infringement action

101 The Claimant is entitled to bring the Infringement action before the Unified Patent Court pursuant Art. 47 (1) UPCA, because the Claimant is deemed to be the proprietor of the patent-in-suit.

102 Pursuant to Rule 8.5 (a) RoP, in relation to the proprietor of a European patent, the person entitled to be registered as proprietor under the law of each Contracting Member State in which such European patent has been validated shall be treated as the proprietor whether or not such person is in fact recorded in the register of patents. However, pursuant to Rule 8.5 (c) RoP, there is a rebuttable presumption that the person shown in each national patent register and the European Patent Register is the person entitled to be registered as proprietor.

103 The rebuttable presumption means that the burden of substantiation and proof now lies with the Defendant. He must substantiate that the Claimant is not the proprietor of the patent-in-suit and that the entry in the register is therefore incorrect. It is not sufficient to simply dispute the ownership of the patent or the effectiveness of a patent assignment. Rather, the Defendant must present specific facts from which it can be concluded that the Claimant is not the patent proprietor.

104 In the case at hand, the Claimant is shown as patent proprietor in the concerned national patent registers (see Exhibit P 4 and P 5) and in the European Patent Register (see Exhibit P 3) and is therefore to be considered the patent proprietor. The Defendants have not successfully rebutted this presumption.

105 Insofar as the Defendants object to the Claimant’s allegedly late submission of documents such as the PPA and the PA (Exhibit P 24 and P 25), this objection is invalid because it is up to the Defendants to present facts that refute the Claimant's ownership of the patent-in-suit. However, the Defendants' further submissions are limited to merely disputing the content of

the agreements, the fulfilment of the contractual conditions for the patent assignment and the signatories' authority to sign the agreements.

106 The only facts pointed out by the Defendants are the different colours and formats of individual pages of the agreements, which suggest that the agreements were composed of different documents or that only signature pages with different formats were exchanged. However, this and the legal opinions expressed by the Defendants on the interpretation of the agreements and the scope of authority of individual signatories do not allow the compelling conclusion that the entire patent assignment is invalid.

107 As the Claimant is considered the patent proprietor, it is in any case entitled to bring the Infringement action. Whether it is also entitled to claims arising from the patent for the period prior to acquisition of the patent-in-suit is, at most, a question of the merits of the action, unless it is already entitled to assert all claims arising from the patent on the basis of its ownership. However, a decision on this point is not necessary here.

B Counterclaim for revocation

108 A decision on the Counterclaim for revocation is not precluded by the fact that the Defendants stated in the oral hearing that they would be willing to condition their counterclaim for revocation to the Infringement question. During the oral hearing, the court merely raised the possibility of a conditional counterclaim for discussion and made it clear that such a conditional counterclaim could be reflected in a corresponding request. However, the possibility of a conditional counterclaim was not discussed further by the parties, no case law was cited if any was known at that time (see Local Division Mannheim, decision of 5 December 2025, UPC_CFI_414/2024), and no formal request was made ("we would be willing …"), in particular, no specific condition was mentioned under which a decision should be made on the counterclaim or not. In this regard, the Defendants' statement at the end of the oral hearing that they want to set the condition is not sufficient.

Part 2: On the merits

109 Both the Counterclaim for revocation and the Infringement action is unfounded

A Subject matter of the patent-in-suit

110 The invention of the patent-in-suit relates to an integrated circuit with a data communication network and an integrated circuit design method.

I. Prior art, problem and solution

111 The patent-in-suit explains that nowadays, most integrated circuits (ICs) are very large scale integration (VLSI) circuits having a large number of features that typically implement a large number of functions on board the IC. The various functions may be located in discrete functional blocks, e.g. system on chip (SoC) architectures. The interconnect of the functional blocks poses a design challenge, because the high clock speeds of modern ICs facilitate the processing of large amounts of data, which means that the interconnect of the IC must be capable of communicating large amounts of data between the functional blocks (para. [0001]; the following citations of paragraphs without reference are those of the patent-in-suit).

112 To facilitate flexible communication on the one hand and to limit the amount of wires required on the other hand, ICs may incorporate a data communication network, also referred to as a network on chip (NoC). Such networks typically comprise a plurality of network stations, each associated with a functional block, interconnected via communication channels, e.g. wires. The plurality of network stations includes a plurality of data routers and a plurality of network interfaces, each data router being coupled to a functional block via a network interface. The data can be communicated over the network in the form of packages that include a mixture of data and routing instructions for the network stations. In networks facilitating duplex communication, a pair of network stations is typically interconnected via at least a pair of communication subchannels to facilitate the two-way communication (para. [0002]).

113 According to the patent in suit, a problem associated with communication channels, e.g. wires, on ICs is that the clock speed at which the IC can operate may be determined by the slowest communication channel, i.e. the channel exhibiting the largest data transfer delay. Several solutions for such a problem exist, see for instance Carloni et al.: Coping with latency in SoC design, IEEE Micro 5, Vol. 22, pages 24-35, IEEE 2002, in which a number of solutions are presented. A possible solution is to introduce a data storage element such as a latch into the slowest data communication channel. Consequently, the clock speed of the data communication part of the IC can be increased at the expense of an additional clock cycle for the communication along the slowest communication channel (para. [0003]).

114 Unfortunately, such a solution cannot straightforwardly be applied to ICs communicating data between the functional blocks via an integrated network, especially when the nature of the communicated data differs per clock cycle; see E. Rijpkema et al.: Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip; IEE Proc.-Comput. Digit. Tech. 2003, page 1-9 (IEE proceedings online no. 20030830), for an example of such a network. Such a network operates on the principle that a network station such as a data router receives the routing data incorporated in the data packet during a predefined clock cycle. Delaying the communication to that router over a slow communication channel by a clock cycle to speed up the rest of the network would cause the routing data to arrive outside the predefined clock cycle, causing erroneous behaviour of the network (para. [0004]).

115 Dielissen J. et al.: "Concepts and Implementation of the Philips Network-on-Chip", in: Internet, 13 November 2003 (2003-11-13), XP002330547, describes a network on chip (NoC) having routers and network interfaces. To reduce queuing capacity of a router, and thus the area, input queuing is used. The router has a controller and a data path. In the data path, the input messages, from either routers or network interfaces are parsed by the header-parsing units (hpu). These units remove the first element for the path, send the parsed flits into guaranteed throughput (GT) or best-effort (BE) queues and notify the controller that there is a packet (para. [0005]).

116 According to Chandra V. et al.: "An interconnect channel design methodology for high performance integrated circuits", at: Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings Feb. 16-20, 2004, Piscataway, NJ, USA, IEEE, vol. 2, 16 February 2004 (2004-02-16), pages 1138-1143, XP010684819 ISBN: 0-7695-2085-5, onchip communication is becoming a bottleneck for high performance designs. Conventional interconnect design methodology does not account for architectures and/or communication schemes that require storage buffers (First-In-First-Out queues or FIFOs) in the interconnect channel. For example, FIFOs and flow-control are needed for Network-on-Chip, high performance ASICs and multiple clock domain designs. These IC implementation architectures require an efficient methodology to determine the size of the FIFOs in the channel since the FIFO sizes affect system performance (para. [0006]).

117 Against this backdrop, it is an objective of the invention (the problem underlying the patent-in-suit) to improve the data communication speed of a network of an integrated circuit having a plurality of functional blocks interconnected via a data communication network (para. [0007]).

118 To solve this problem, the patent-in-suit provides, among other things, an integrated circuit with the features of claim 1, which can be structured as follows:

1. An integrated circuit (10) comprising:
   - 1.1 a plurality of functional blocks (101, 102, 103, 104); and
   - 1.2 a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140);
2. the plurality of network stations
   - 2.1 is interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104);
     - 2.1.1 each data package comprises N data elements
     - 2.1.2 including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140),
     - 2.1.3 N being an integer of at least two;
   - 2.2 comprises a plurality of network interfaces (105-108);

2.3 comprises a plurality of data routers (110, 120, 130, 140), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108);

3. the data communication network (100) comprises a first data router (140) and a second data router (120) interconnected through a first communication channel (150);

4. the first communication channel (150) comprises M*N data storage elements (160), (M.1.8)

4.1 M being a positive integer,

4.2 for delaying whole data packages including the routing information by introducing a delay of M*N cycles on the first communication channel (150).

119 Furthermore, the patent-in-suit suggests a method of designing an integrated circuit with the features of claim 8 which can be structured as follows:

1. A method of designing an integrated circuit (10)

1.1 a plurality of functional blocks (101, 102, 103, 104); and

1.2 a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140);

2. the plurality of network stations

2.1 is interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104);

2.1.1 each data package comprises N data elements

2.1.2 including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140),

2.1.3 N being an integer of at least two;

2.2 comprises a plurality of network interfaces (105-108);

2.3 comprises a plurality of data routers (110, 120, 130, 140), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108);

3. the method comprises:

3.1 identifying a first communication channel (150) between a first data router (140) and a second data router (120) that has a data transfer delay exceeding a predefined delay threshold; and

3.2 inserting M*N data storage elements (160) into the first communication channel (150), M being a positive integer, for delaying whole data packages

including the routing information by introducing a delay of M*N cycles on the first communication channel (150).

II. Claim construction

In view of the dispute of the parties, the interpretation of the claims is necessary, in particular with regard to the features 2.1.1 to 2.1.3 and feature group 4 of claim 1, and features 2.1.1 to 2.1.3 and feature group 3 of claim 8, respectively. Unless otherwise stated, the claim interpretation refers to claim 1 and also applies to claim 8 as the relevant features are identical.

1. Legal framework for claim interpretation

120 In accordance with Art. 69 (1) EPC and the Protocol on its interpretation, a patent claim is not only the starting point, but the decisive basis for determining the scope of protection of a European patent. The interpretation of a patent claim does not depend solely on the strict, literal meaning of the wording used. Rather, the description and the drawings must always be used as explanatory aids for the interpretation of the patent claim and not only to resolve any ambiguities in the patent claim. However, this does not mean that the patent claim merely serves as a guideline and that its subject-matter also extends to what, after examination of the description and drawings, appears to be the subject-matter for which the patent proprietor seeks protection (Court of Appeal, UPC_CoA_335/2023, Decision of 26 February 2023 in conjunction with Decision of 11 March 2024 – NanoString v 10x Genomics; UPC_CoA_1/2024, Order of 13 May 2024 – VusionGroup v Hanshow; UPC_CoA_768/2024, Order of 30 April 2025 – Insulet v EOFlow, UPC_CoA_405/2024, 19 June 2025 – Alexion/Amgen; UPC_CoA_579/2025, Order of 7 November 2025 – OTEC/STEROS). Rather, Art. 69 EPC and its Protocol establish a primacy of the claims. The underlying legal principle is legal certainty.

121 These principles for interpreting a patent claim apply both to the question of patent infringement and to the question of validity. The understanding of a claim by the skilled person must be consistent for all purposes of the evaluation of infringement and validity (Court of Appeal, UPC_CoA_335/2023, Order of 26 February 2024 – NanoString v 10x Genomics).

2. Case at hand

Based on these principles, the following applies in the present case.

a) Skilled person

122 The skilled person is to be defined as an electrical engineer or computer scientist with practical experience in the field of SoC and NoC technologies and with general notions of computer networks and with basic knowledge of electrical engineering or computer engineering acquired as part of his/her studies. This definition largely corresponds to the definition suggested by the

Claimant. However, insofar as Claimant argues that the skilled person would not be a specialist in, for example, computer networks, this is not convincing. The Defendants have rightly pointed out that the terminology used for NoC such as network, router, network interface, routing information and the like makes it clear that both technical fields overlap considerably. The basic idea of NoC architecture is even borrowed from traditional large-scale multi-processors and the wide-area networks domain (see p. 19 of Exhibit BP-CR 1). Therefore, it can be expected that the skilled person specialised in NoCs has at least general knowledge in the field of computer networks.

b) General claim structure

123 Claim 1 relates to an integrated circuit comprising a plurality of functional blocks and a data communication network comprising a plurality of network stations (feature group 1). The relation between functional blocks and network stations is described as the network stations comprising a plurality of data routers and network interfaces whereby each of the data routers is coupled to a functional block via a network interface (features 2.2 and 2.3). The functional blocks send and receive data packages. To this end, the plurality of network stations is interconnected via a plurality of communication channels for communicating the data packages between the functional blocks (feature 2.1).

124 This integrated circuit arrangement was generally known in prior art (cf. para. [0002]) and requires no further explanation. The particularities relate to the structure of the data packages and the delay in the transmission of such data packages, i.e. features 2.1.1 to 2.1.3 and feature group 4.

c) Feature group 2.1

125 The features 2.1.1 to 2.1.3 are to be understood in the sense that the data package is a unit of data provided with routing information, which is communicated between the functional blocks and, without exception, has a fixed size of N data elements, with N being an integer of at least 2. A data element is the unit that is transmitted during one clock cycle between two network stations. In addition, the routing information must be contained in one of the data elements of each data package. This understanding can be derived from the wording of feature group 2.1, its interplay with feature group 4, the description of the patent-in-suit and the technical problem to be solved.

(1)

126 According to the clear wording of claim 1, data packages are communicated between the functional blocks and each data package must comprise N data elements. Thereby, N is a specific integer which cannot vary from data package to data package but applies in principle to the entire network or at least part of the network. This already follows from feature group 4, according to which the first communication channel must comprise M*N elements. Since this

is hardware that is already specified when designing the IC, N cannot vary either. Hence, all data packages must also have a fixed size of N data elements.

127 A data element is the amount of data transferred during one clock cycle between two network stations. This can also be derived from feature group 4. If M = 1, the first communication channel comprises N data storage element, i.e. as many as data elements are comprised by a data package (cf. feature 4). These N data storage elements provide for a delay of the whole data package, i.e. N data elements, by introducing a delay of N cycles on the first communication channel (feature 4.2). Since the skilled person endeavours to give the technical teaching a meaningful interpretation, delaying an entire data package with N data elements by N clock cycles necessarily requires that one data element is transferred per clock cycle.

128 Against this background, the requirements of features 2.1.1 to 2.1.3 are not met if any data package, regardless of the packets in which it is transmitted, is simply divided into N parts that are considered data elements – even if the number N of parts corresponds to the number of data storage elements in the first communication channel or a multiple thereof, unless one data element per clock cycle is transmitted. In particular, data packages cannot be arbitrarily grouped in N units of data that are considered data elements. Rather, a data element is a fixed unit of data that is transmitted during one clock cycle, and each data package must comprise exactly N of these data elements. In this regard, a data element is not necessarily an undefined amount of data, but will be a meaningful unit, at least as far as routing information is concerned. This is because one data element of every data package must contain routing information (feature 2.1.2).

129 Consequently, the data package itself is regularly a meaningful data unit transferred between the functional blocks as it contains routing information in one of its data elements. Typically, a data package is the data packet provided for in the network protocol that contains a header with routing information and payload. In this regard, there is no difference between the terms “data package” and “data packet”. Even the patent-in-suit uses the terms synonymously and interchangeably (cf. [0004])

(2)

130 This understanding of the features 2.1.1 to 2.1.3 is confirmed by the description of the patent-in-suit.

131 When interpreting these features, it has to be taken into account, that, according to the description of the patent-in-suit, “the invention is based on the realisation that the correct operation of the network relies on the maintenance of the correct periodicity between the network stations” (para. [0008]). That means that the basis for the technical teaching of the patent and the starting point for the skilled person’s considerations is not just any network on chip but a network (or IC) that implies periodicity of data transmission between the network stations.

132 According to the patent specification, the invention of the patent-in-suit aims to improve the data communication speed of a network of an IC (para. [0007]). The patent specification describes a problem associated with the communication channels on ICs in that the clock speed at which the IC can operate may be determined by the slowest communication channel. However, according to the patent description, several solutions for such a problem exist in prior art. As an example, introducing a data storage element such as a latch into the slowest data communication channel is one possible solution. The clock speed of the data communication part of the IC can be increased at the expense of an additional clock cycle for the communication along the slowest communication channel. (para. [0003]).

133 The technical problem addressed by the patent-in-suit is therefore more specific and arises from ICs which communicate data between the functional blocks via an integrated network to which the more general solution known in the art cannot straightforwardly be applied. These networks are characterised in that they operate on the principle that a network station such as a router receives the routing data incorporated in the data packet during a predefined clock cycle (para. [0004]). The router is dependent on receiving data such as routing information at a specific clock cycle. Delaying communication to that router over a slow communication channel by only one clock cycle, as is known in the art, would cause the routing data to arrive outside the predefined clock cycle, causing erroneous behaviour of the network (para. [0004]).

134 From this it immediately becomes clear what is meant by “periodicity between network stations” (para. [0008]) and each data package comprising N data elements (feature 2.1.1). Even if the data communicated in these “specific networks” differs per clock cycle (see para. [0004]), certain data such as routing information can be expected and received by a network station during a specific clock cycle because it is periodically transferred. This requires that each data package – understood as a meaningful unit to be transmitted between functional blocks and therefore containing routing information – comprises exactly N data elements. As one data element is transmitted per clock cycle, the entire data packet is transmitted after N clock cycles. If the data element comprising the routing information is located at a predetermined position in the data package, the network station receives this information every Nth clock cycle, thus periodically.

135 This is also explicitly described in the patent specification:

> “The invention is based on the realization that the correct operation of the network relies on the maintenance of the correct periodicity between the network stations. Because the data packages have a fixed size of N data elements, the communication of a complete package between two network stations takes N clock cycles, or N handshake driven data transfers in case of an asynchronous implementation of the network. The routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain such information.” (para. [0008])

136 The patent-in-suit, and in particular claim 1 with features 2.1.1 and 2.1.3, therefore necessarily require that each data package communicated between the functional blocks comprises exactly N data elements, with exactly one data element being transmitted per clock cycle, so that the data packages can be transmitted periodically and – if the data element with the routing information is located at a predetermined position in the data package – the routing information is transmitted every Nth clock cycle. This is nothing new, features 2.1.1 to 2.1.3 simply describe the structure of data and data packets that are transmitted in a network whose network stations depend on periodicity, as was known in prior art.

137 Even if claim 1 does not contain any specific requirements, the patent description specifies that the routing information has a fixed position in the data package, e.g. the first data element, although other data elements may (also) contain such information (para. [0008]). However, it is necessary according to feature 2.1.1 to 2.1.3 that the data packets contain exactly N data elements and that, consequently, the routing information has a fixed position, so that a corresponding network requiring periodicity can properly operate, since it expects routing information to arrive periodically after every N cycles.

d) Feature group 4

138 The IC according to the invention differs from the prior art precisely in feature group 4.

139 The arrangement of M*N data storage elements in one of the data communication channels between two data routers (features 4) – also referred to as the first data communication channel (feature 3) – M being a positive integer (feature 4.1), has the function of delaying the transmission of an entire data package, including the routing information, by M*N clock cycles (feature 4.2). This function of the M*N data elements is explicitly mentioned in feature 4.2 of claim 1 (“for”). Since the data package comprises N data elements, one data element is transmitted per clock cycle, and M*N is a multiple of N, the arrangement of M*N data storage elements in the communication channel always provides for a delay of the whole data package transmitted thereon by M*N clock cycles.

140 Feature group 4 of the IC is decisive for solving the technical problem addressed in the patent specification. As already mentioned, the problem that the clock speed at which the IC can operate is determined by the slowest communication channel was already solved in the prior art by introducing a data storage element such as a latch into the slowest communication channel and, consequently, increasing the clock speed of the data communication part of the IC at the expense of an additional clock cycle along the slowest communication channel (para. [0003]). However, this solution cannot straightforwardly be applied to ICs whose network implies periodicity between the network stations (para [0004]). It is immediately clear that, if data packets with more than one data element are transferred, a delay of one clock cycle causes the routing data to arrive outside the predefined clock cycle, causing erroneous behaviour of the network (para. [0004]).

141 The objective specified by the patent-in-suit, namely to improve the data communication speed of network, relates precisely to this technical problem in those specific networks. It is solved by delaying the transmission of data packages on the slow communication channel by a whole data package rather than by a single data element. This ensures periodicity between the network stations because the respective information in each data element – such as routing information – is delayed so that it is received at the predefined time.

142 This is also explicitly explained in the patent specification:

> "Since a network station expects routing information to arrive periodically (i.e. after every N cycles), the introduction of a delay on the first communication channel (which typically is the slowest channel of the network) matching such a period, i.e. by delaying the whole data package rather than a single data element, the delayed data package is received by the receiving network station during the appropriate period, e.g. clock cycle." (para. [0008])

143 However, in view of the preferred embodiments and the dependent claims, it must be noted that the purpose to maintain the periodicity of the network does not necessarily mean that all data routers of the network expect the routing information at the same clock cycle. On the contrary, figure 2 and 4 and the dependent claims of the patent-in-suit show that a phase shift between two data routers is allowed and that this phase shift may even be smaller than the number of data elements N (e.g. para. [0027] and fig. 3 and 4). This means that the periodicity of two routers may be offset and the offset is smaller than N, for example because fewer than N data storage elements are inserted in a channel for data packages to be transmitted from router A to router B. In order to nevertheless ensure the periodicity within the individual router, for example in router A when router B immediately sends back a response data package, the sum of the number of data storage elements within the channels for the incoming and outgoing data packets between two routers must be M*N (e.g. paragraphs [0026], [0027], [0029] and dependent claims). The patent-in-suit refers to these channels as "subchannels" whereas one subchannel for incoming data packages and another subchannel for outgoing data packages are comprised by the communication channel within the meaning of feature 4. It must be noted that the individual subchannels do not each constitute the communication channel within the meaning of features 2.1 and 4, and even less so a subnetwork. Even if there is a phase shift between two routers, periodicity within a router must be ensured by the communication channel having a total of M*N data storage elements. Accordingly, all data packets transmitted between these routers must also have the same number of N data elements.

B Counterclaim for revocation

The Counterclaim for revocation is unfounded.

I. Inadmissible amendment of the independent claims

144 The patent-in-suit is not inadmissibly extended within the meaning of Art. 138 (1) (c), 123 (2) EPC and cannot therefore be revoked on this ground pursuant to Article 65 (2) UPCA.

1. Legal principles re. “added matter”

145 In accordance with Art. 65 (2) UPCA in conjunction with Art. 138 (1) (c) EPC, a European patent may be revoked if its subject-matter extends beyond the content of the application as filed or, if the patent was granted on a divisional application or on a new application filed under Art. 61 EPC, beyond the content of the earlier application as filed (added matter).

146 In order to ascertain whether there is added matter, the Court must ascertain what the skilled person would derive directly and unambiguously using his/her common general knowledge and seen objectively and relative to the date of filing, from the whole of the application as filed, whereby implicitly disclosed subject-matter, i.e. matter that is a clear and unambiguous consequence of what is explicitly mentioned, shall also be considered as part of its content (Court of Appeal, Decision of 2 October 2025, UPC_CoA_764/2024 and UPC_CoA_774/2024 – expert e-Commerce/Seoul Viosys; Decision of 14 February, UPC_CoA_382/2024 – Abbott/Sibio; Decision of 25 November 2025, UPC_CoA_528/2024 and UPC_CoA_529/2024 – Sanofi/Amgen)

147 The underlying rationale for this requirement is that the patentee cannot claim more than he actually contributed to the state of the art at the priority date. Therefore, an amendment that is made after the priority date should not provide the skilled person with additional technically relevant information which was not derivable from the original application (Court of Appeal, Decision of 25 November 2025, UPC_CoA_528/2024 and UPC_CoA_529/2024 – Sanofi/Amgen).

148 Where the patent results from a divisional application, this requirement applies to each earlier application. The subject matter of the granted claim thus may not extend beyond (1) the disclosure of the application as filed for the patent in suit and (2) the disclosure of the original PCT application that entered the regional phase and is the parent application for the divisional application (Court of Appeal, Decision of 2 October 2025, UPC_CoA_764/2024 and UPC_CoA_774/2024 – expert e-Commerce/Seoul Viosys).

149 The assessment of whether there is added matter is a question of law to be decided on the basis of the facts brought forward by the parties. The facts are the relevant claims and the application as filed. Since the test is whether the relevant claims have basis in the application as a whole, the Court is allowed to look at the entire document (Court of Appeal, Decision of 25 November 2025, UPC_CoA_528/2024 and UPC_CoA_529/2024 – Sanofi/Amgen).

150 The burden of presentation and proof lies with the party invoking invalidity of the patent (see with regard to sufficient disclosure: Court of Appeal, Decision of 25 November 2025, UPC_CoA_528/2024 and UPC_CoA_529/2024 – Sanofi/Amgen).

2. Present case

151 The subject matter of claims 1 and 8 of the patent-in-suit does not extend beyond the content of the patent application.

152 The Defendants' objection that the amendment of claims 1 and 8 during the examination phase constitutes an inadmissible intermediate generalisation of what is described in the original patent application cannot be accepted. The Defendants argue that the original patent application describes that, in order to maintain the correct periodicity, it is necessary that a complete data package is transmitted within N clock cycles and a whole data package is delayed by N clock cycles. Only the latter feature was included in the claims. Without the limitation that a complete data package is transmitted within N clock cycles, it would not be technically possible to ensure that the correct periodicity between network stations is maintained. However, this is not correct.

153 As explained in the section "claim construction", the term "data element" in the patent-in-suit has to be understood as the unit of data which is transmitted during one clock cycle. From this and the requirement that a whole data package including the routing information must be delayed by introducing a delay of M*N cycles on the first communication channel, it can be derived that the whole data package must be transmitted within N clock cycles. This also follows from the basic assumption of the patent-in-suit that periodicity must be maintained although a delay of communication is inserted. Finally, the patent explicitly mentions that the transfer of a complete data packet requires N clock cycles (para. [0008]). Even though this is not explicitly included in the claims, according to the teaching of the patent-in-suit, the objective of improving the clock speed while maintaining periodicity can only be achieved if the whole data package with the N data elements is delayed by N clock cycles or a multiple thereof, which necessarily presupposes that the complete data package is transmitted within these N clock cycles. The fact that the latter is not expressly mentioned in the claims is irrelevant, as it follows from a correct interpretation anyway. The lack of mention in the claim does not mean that periodicity is lost. Rather, the maintenance of periodicity as the objective of the patent-in-suit requires the complete data package to be transmitted within N clock cycles. This is recognised by the skilled person who endeavours to interpret the claim in a technically meaningful way. Anything else would be an artificial interpretation.

154 All of this is actually already apparent from the Defendant's own statements in the Counterclaim for revocation, where it reads: "For example, if less than all N data elements of a data package are transmitted onto the communication channel during the delay of M*N clock cycles introduced by the M*N data storage elements, it is technically not possible to delay the whole data package" (mn. 9 of the Counterclaim for revocation). This is true, and precisely

because delaying the whole data package would not be possible in such a case but is required by claims 1 and 8 (feature 4.2 of claim 1 and 3.2 of claim 8), the complete data package must be transmitted in N clock cycles. In the Reply to the Defense to the Counterclaim, the Defendants rely on alleged differences between data packages and data packets. However, the patent-in-suit does not differentiate between these terms and there is no reason to introduce the data packet as a further data unit that can only be arbitrarily distinguished from the data package.

155 As a result, the subject matter of claims 1 and 8 does not extend beyond the content of the original patent application. In particular, the amendment of the claims during the examination phase does not constitute an inadmissible intermediate generalization. The claims implicitly require the complete data package to be transmitted within N clock cycles.

II. Patentability

156 The teaching of the patent-in-suit is novel and inventive pursuant to Art. 54 and 56 EPC.

1. Novelty re. BP-CR 1/“Bertozzi“

157 The subject matter of patent claims 1 and 8 is novel over Bertozzi et al., “Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-Chip”, published on 3 September 2004 in IEEE Circuits and Systems Magazine (Vol. 4, Issue 2, 2004) (hereinafter: “Bertozzi”).

a) Legal principles

158 As already clarified in UPC case law, it is a prerequisite for the acceptance of lack of novelty that the claimed subject matter is directly and unambiguously derivable from the prior art. The technical disclosure in a prior art document must be considered as a whole (CoA, Order of 25 September 2024, UPC_CoA_182/2024, para. 123). The Court must ascertain what the skilled person would derive directly and unambiguously using his/her common general knowledge and seen objectively and relative to the date of filing, from the whole of the prior art document, whereby implicitly disclosed subject-matter, i.e. matter that is a clear and unambiguous consequence of what is explicitly mentioned, shall also be considered as part of its content (see with regard to added matter: Court of Appeal, 2 October 2025, UPC_CoA_764/2024, UPC_CoA_774/2024 – expert e-Commerce/Seoul Viosys; 14 February 2025, UPC_CoA_382/2024 – Abbott/Sibio). An invention is to be considered part of the state of the art when it is found clearly integrally, directly and unambiguously in one single piece of prior art and it is identical in its constituent elements, in the same form, with the same arrangement and the same features (LD Munich, Decision of 31 July 2024, UPC_CFI_233/2023; CD Paris, Decision of 28 July 2025, UPC_CFI_239/2024). This principle applies also when a novelty attack is based on a single piece of prior art made available to the public by use (LD Milan, Decision of 27 October 2025, UPC_CFI_178/2024 and UPC_CFI_432/2024).

b) Case at hand

159 „Bertozzi“ relates to a Network-on-Chip Architecture. The article introduces an advanced NoC architecture, called Xpipes, targeting high performance and reliable communication for on-chip multi-processors. It consists of a library of soft macros (switches, network interfaces and links) that are design-time composable and tunable so that domain-specific heterogeneous architectures can be instantiated and synthesized. In particular, the article also deals with links which are pipelined to decouple link throughput from its length and to get arbitrary topologies (see p. 18 “Abstract” of „Bertozzi“).

160 An example of Network-on-Chip architecture according to „Bertozzi“ is illustrated below:

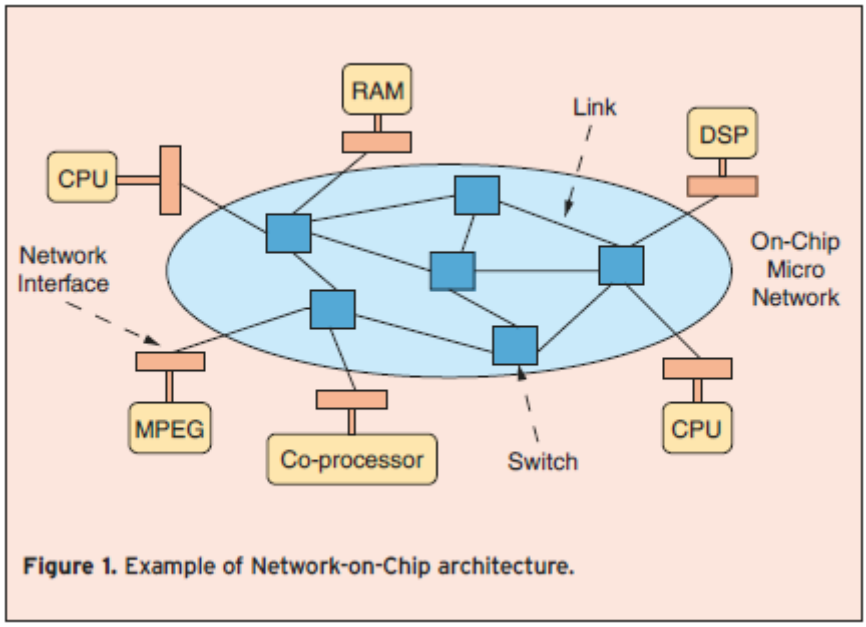

Figure 1. Example of Network-on-Chip architecture.

161 The parties rightly agree that the NoC architecture described in “Bertozzi” discloses features 1 to 3 of patent claim 1 and features 1 to 3.1 of patent claim 8, respectively. In particular, „Bertozzi“ describes data packages in the form of messages according features 2.1.1 to 2.1.3 of patent claims 1 and 8:

> “Messages that have to be transmitted across the network are usually partitioned into fixed-length packets. Packets in turn are often broken into message flow control units called *flits*. In the presence of channel width constraints, multiple physical channel cycles can be used to transfer a single flit. A *phit* is the unit of information that can be transferred across a physical channel in a single step. Flits represent logical units of information, as opposed to phits that correspond to physical quantities. In many implementations, a flit is set to be equal to a phit. The packet preparation process consists of building the packet header, payload and packet tail. The header contains the necessary routing and network control information.” (p. 22, left. col., 4th para. of „Bertozzi“)

162 The packet partitioning is depicted below as an example from „Bertozzi“. In this example, the packets have fixed size of 10 flits which can be considered as data elements within the meaning of the patent-in-suit:

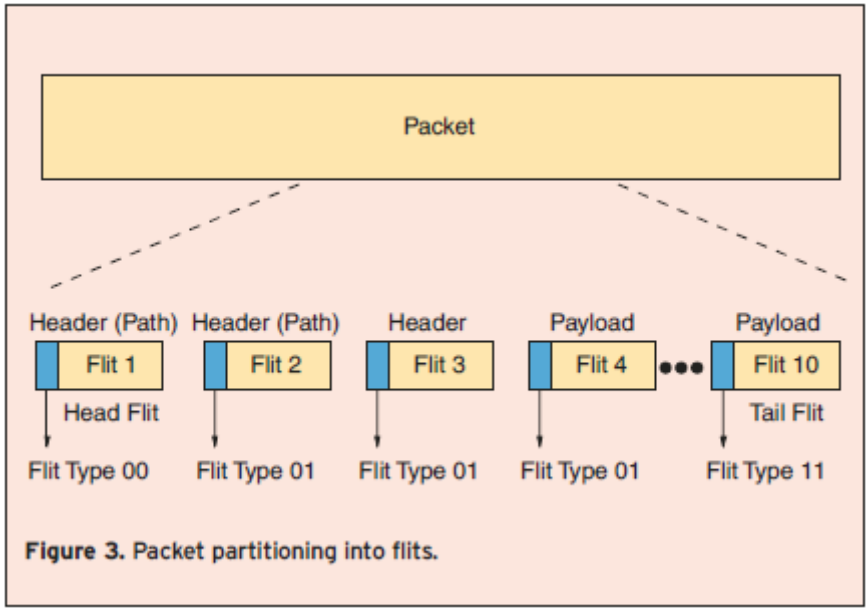

Figure 3. Packet partitioning into flits.

163 However, feature group 4 of patent claim 1 and feature 3.2 of patent claim 8 are not disclosed. In „Bertozzi“, there is no indication – either explicit or implicit – that the number of data storage elements in a data communication channel correlates in any way with the number of data elements contained in a data package. Rather, the number of data storage elements depends on the desired length of each segment of a link.

164 The Defendants correctly point out that „Bertozzi“ identifies the technical problem that

> “the design of communication (switch-to-switch and network interface-to-switch) links represents a critical issue with respect to the system performance. As geometries shrink, gate delay improves much faster than the delay in long wires. Therefore, the long wires increasingly determine the maximum clock rate, and hence performance, of the entire design. [...] Techniques have to be devised to decouple link throughput from its length and to allow functionally correct operation of the switches in presence of misaligned inputs due to the unequal length of the input links” (p. 23, left col. 2nd para. of „Bertozzi“)

165 According to „Bertozzi“

> ““a solution to overcome the interconnect-delay problem consists of pipelining interconnects [34, 35]. Wires can be partitioned into segments (or relay stations, which have a function similar to the one of latches in a pipelined data path) whose length satisfies predefined timing requirements (e.g., the desired clock speed of the design). In this way, link delay is changed into latency, but the data introduction rate is not bound by

the link delay any more. (…) This requires the system to be composed of modules whose behavior does not depend on the latency of input communication channels." (p. 24, right col., 3rd para. of „Bertozzi")

166 It cannot be inferred from these passages that the number of relay stations or latches, which partition the wires into segments, correlates with the number of flits in a packet within the meaning of features 4 and 4.1 of claim 1 or feature 3.1 of claim 8. A delay of a whole data packet within the meaning of feature 4.2 of claim 1 or feature 3.2 of claim 8 is also not required. On the contrary, the citations indicate that the length of the segments is to satisfy pre-defined timing requirements. Elsewhere, it is even stated that the length of the link segments can be tailored to the desired clock frequency that needs to be achieved in the design (p. 24, right col., last para. of „Bertozzi"), and that the number of pipeline stages for each link is also determined based on the clock speed target and link routing (p. 29, left col. 2nd para. of „Bertozzi"). In contrast, no relationship of the pipeline stages to the number of flits or data elements in a data packet is disclosed.

167 The Defendants primarily refer to figure 4 of „Bertozzi", which is shown below, to justify their opinion.

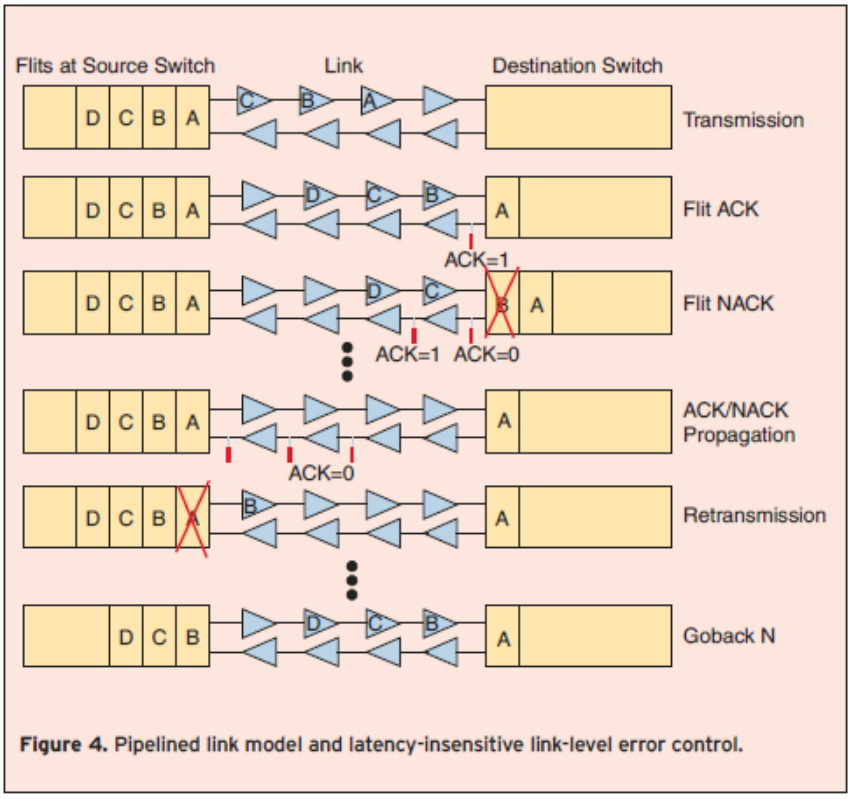

Figure 4. Pipelined link model and latency-insensitive link-level error control.

This figure shows four flits A to D and four relay or repeater stages in each direction between two switches. The relay stations also insert a delay of N clock cycles where N is the link length expressed in terms of number or repeater stages (p. 25, left col., 2nd para. of „Bertozzi").

168 However, figure 4 is a schematic pipelined link model that makes no claim to accuracy with regard to the number of repeater stages and the number of flits in a data packet, and even less so with regard to the correlation of both values. Even though four flits are shown with A to D, this does not mean that the data packet consists of only four flits and the number of repeater stages must be equal to the number of flits in a data packet. It is even possible that the four flits must be attributed to different data packets. The numbering from A to D distinguishes between four flits but does not indicate which data packet they belong to. Figure 4 does not deal with the structure of data packets, the number of flits contained in a data packet and the number of repeater stages. On the other hand, figure 3 of „Bertozzi“, already shown above, reveals the structure and partitioning of a complete data packet. According to this, a data packet comprises ten flits so that it is ruled out or at least merely not disclosed that the four flits A to D in figure 4 of „Bertozzi“ form a data packet. Therefore, “Bertozzi” explains figure 4 and the number of flits only in that “multiple outstanding flits propagate across the link during the same clock cycle” (p. 25, left col., 2nd para. of “Bertozzi”). This does not allow any conclusions to be drawn about the number of flits in a data packet and their relationship to the number of pipeline stages as “outstanding flits” do not preclude further flits of a data packet from having already been transmitted. The same applies to the fact that the fields behind flit D in figure 4 stay empty. This can be understood to mean that there is a plurality of other flits after flit D, which are not shown for explanatory reasons, as figure 4 does not refer to the communication of a whole data packet. The defendant's reasoning as to why Flits A to D should constitute a complete data package is based on mere assumptions made in hindsight.

169 Even if the number of repeater stages in figure 4 of „Bertozzi“ corresponds to the number of flits and even if it is assumed that these four flits A to D in figure 4 form a data packet, the skilled person would not understand this coincidental connection to mean that a first communication channel in a NoC must comprise as many repeater stages as flits are contained in a data packet or a multiple thereof. It is not directly and unambiguously disclosed that this relation between the number of flits and the number of repeater stages is part of the technical teaching disclosed in „Bertozzi“. On the contrary, the disclosure content of „Bertozzi“ otherwise indicates that the number of repeater stages does not have to correspond to the number of flits or a multiple thereof, and Figure 4 must also be understood in this way.

170 Unlike the patent-in-suit, „Bertozzi“ does not aim to increase the clock speed while maintaining the correct periodicity as the network stations expect routing information to arrive within predefined evaluation cycles (para. [0008]). On the contrary, as the Claimant points out, „Bertozzi“ expressly states that switch operation is latency insensitive, in that correct operation is guaranteed for arbitrary link pipeline depth (p. 25, right col. 1st para. of „Bertozzi“). There is no reason to believe that the “multiple outstanding flits” equate exactly to N flits, “where N is the link length expressed in terms of number of repeater stages” (p. 25, right col. 2nd para. of „Bertozzi“). In addition, according to the abstract of „Bertozzi“, an arbitrary amount of repeater stages can be inserted into a communication channel as it reads:

> “Links can be pipelined with a flexible number of stages to decouple link throughput from its length and to get arbitrary topologies.” (p. 18 “Abstract” of „Bertozzi“).

The number of repeater stages and the length of links only depend on the pre-defined timing requirements (p. 24, right col, 3rd para. of „Bertozzi“), not the periodicity between network stations. Accordingly, „Bertozzi“ requires that the switches must operate correctly for any arbitrary number of repeater stages on a link, i.e. for routing information that arrives at a destination switch in any cycle rather than in only predefined evaluation cycles as required by the patent-in-suit (see also the already quoted passage on p. 24, right col., 3rd para. of „Bertozzi“). Bertozzi even gives an idea of how the switch can still determine the correct start and end of a data packet and thereby maintain periodicity. Since the last flit of a data packet is explicitly designated as a “tail flit” (see figure 3), which marks the end of the data packet, a switch can use this to recognise the end of the data packet and, due to the fixed length, also the first flit of the data packet.

171 As a result, „Bertozzi“ does not disclose feature group 4 of patent claim 1 and feature 3.2 of patent claim 8, if it does not even exclude this technical teaching.

2. Inventive step

172 The invention under claim 1 of the patent-in-suit is not obvious to a person skilled in the art from the prior art.

a) Legal principles

173 Pursuant to Art. 56 EPC, an invention is considered to involve an inventive step if it is not obvious to a person skilled in the art from the prior art. This is always a question of the individual case and requires examination considering all relevant facts and circumstances.

174 The approach taken by the Unified Patent Court when establishing inventive step is as follows:

175 It first has to be established what the object of the invention is, i.e. the objective problem. In order to avoid hindsight, the objective problem should not contain pointers to the claimed solution (Court of Appeal, Decision of 25 November 2025, UPC_CFI_528/2024 and UPC_CFI_529/2024 – Sanofi/Amgen)

176 This must be assessed from the perspective of the skilled person, with its common general knowledge, as at the application or priority date (also referred to as the relevant date) of the patent. This must be done by establishing what the invention adds to the state of the art, not by looking at the individual features of the claim, but by comparing the claim as a whole in context of the description and the drawings, thus also considering the inventive concept underlying the invention (the technical teaching), which must be based on the technical effect(s) that the skilled person on the basis of the patent understands is (are) achieved with the claimed invention (Court of Appeal, Decision of 25 November 2025, UPC_CFI_528/2024

and UPC_CFI_529/2024 – Sanofi/Amgen; Decision of 25 November, UPC_CFI_464/2024 and UPC_CFI_530/2024 – Meril/Edwards).

177 The claimed solution is obvious when at the relevant date the skilled person, starting from a realistic starting point in the state of the art in the relevant field of technology, wishing to solve the objective problem, *would* (and not only: *could*) have arrived at the claimed solution (Court of Appeal, Decision of 25 November 2025, UPC_CFI_528/2024 and UPC_CFI_529/2024 – Sanofi/Amgen; Decision of 25 November, UPC_CFI_464/2024 and UPC_CFI_530/2024 – Meril/Edwards).

178 The relevant field of technology is the field relevant to the objective problem to be solved as well as any field in which the same or similar problem arises and of which the person skilled in the art of the specific field must be expected to be aware (Court of Appeal, Decision of 25 November 2025, UPC_CFI_528/2024 and UPC_CFI_529/2024 – Sanofi/Amgen; Decision of 25 November, UPC_CFI_464/2024 and UPC_CFI_530/2024 – Meril/Edwards).

179 A starting point is realistic if the teaching thereof would have been of interest to a skilled person who, at the relevant date, wishes to solve the objective problem. This may for instance be the case if the relevant piece of prior art already discloses several features similar to those relevant to the invention as claimed and/or addresses the same or a similar underlying problem as that of the claimed invention. There can be more than one realistic starting point and the claimed invention must be inventive starting from each of them (Court of Appeal, Decision of 25 November 2025, UPC_CoA_528/2024 and UPC_CoA_529/2024 – Sanofi/Amgen; Decision of 25 November, UPC_CFI_464/2024 and UPC_CFI_530/2024 – Meril/Edwards; Order of 26 February 2024, UPC-CoA_335/2023; CD Munich, Decision of 16 July 2024, UPC_CFI_1/2023; Decision of 17 October 2024, UPC_CFI_252/2023; CD Paris, Decision of 26 December 2024, UPC_CFI_338/2023 and UPC_CFI_410/2023; LD Düsseldorf, Decision of 10 April 2025, UPC_CFI_50/2024; LD Hamburg, UPC_CFI_173/2024 and 424/2024, Decision of 10 July 2025). There may be several realistic starting points. It is not necessary to determine the 'most promising' starting point (CD Munich, Decision of 16 July 2024, UPC_CFI_1/2023; CD Munich, Decision of 17 October 2024, UPC_CFI_252/2023; CD Paris, Decision of 5 November 2024, UPC_CFI_315/2024; CD Paris, Decision of 26 December 2024, UPC_CFI_338/2023 UPC_CFI_410/2023 LD Mannheim, UPC_CFI_340/2023, 31 January 2025; LD Munich (Panel 2), UPC_CFI_248/2024, 22. August 2025 – Brita/Aquashield).

180 The skilled person has no inventive skills and no imagination and requires a pointer or motivation that, starting from a realistic starting point, directs it to implement a next step in the direction of the claimed invention. As a general rule, a claimed solution must be considered not inventive / obvious when the skilled person would take the next step prompted by the pointer or as a matter of routine and arrive at the claimed invention (Court of Appeal, Decision of 25 November 2025, UPC_CFI_528/2024 and UPC_CFI_529/2024 – Sanofi/Amgen; Decision of 25 November, UPC_CFI_464/2024 and UPC_CFI_530/2024 – Meril/Edwards; Order of 26 February 2024, UPC_CoA_335/2023; CD Munich, Decision of 16 July 2024,

UPC_CFI_1/2023; Decision of 17 October 2024, UPC_CFI_252/2023; LD Düsseldorf, Decision of 10 October 2024, UPC_CFI_363/2023; Decision of 10 April 2025, UPC_CFI_50/2024; LD Mannheim, Decision of 2 April 2025, UPC_CFI_365/2023).

181 A claimed solution is obvious if the skilled person would have taken the next step in expectation of finding an envisaged solution of his technical problem (Court of Appeal, Decision of 25 November 2025, UPC_CFI_528/2024 and UPC_CFI_529/2024 – Sanofi/Amgen).

182 The burden and presentation of proof with regard to the facts from which the lack of validity of the patent is derived and other circumstances favourable to the invalidity or revocation lies with the claimant in a revocation action. Therefore, the burden of proof that the results were clearly predictable or the skilled person would have reasonably expected success, i.e. that the solution he envisages by taking the next step would solve the objective problem, lies as well on the party asserting invalidity of the patent. Even though proof of certain facts, if contested, may be required, the assessment of whether the legal consequence for which the facts and circumstances have been submitted is justified, is a question of law (Court of Appeal, Decision of 25 November 2025, UPC_CFI_528/2024 and UPC_CFI_529/2024 – Sanofi/Amgen; Decision of 25 November, UPC_CFI_464/2024 and UPC_CFI_530/2024 – Meril/Edwards).

b) BP-CR 1 (“Bertozzi”) in combination with BP-CR 2 (“Nowatzyk”)

183 The technical teaching according to patent claims 1 and 8 is not obvious to a person skilled in the art from “Bertozzi“ (BP-CR 1) in combination with the US patent US 6,081,844, published on 27 June 2000 (BP-CR 2; hereinafter: „Nowatzyk“).

(1)

184 As elaborated in the context of claim interpretation, the objective problem underlying the technical teaching of patent claims 1 and 8 is the improvement of the clock speed in relation to networks on chip which must maintain a correct periodicity between the network stations. “Bertozzi” is not a suitable starting point in the prior art for solving this problem because it does not refer to such NoCs. Even if it is considered a starting point, for the same reasons, “Bertozzi” does not contain any pointer or incentive for the skilled person directing him in the direction of the claimed invention.

185 “Bertozzi“ offers no incentive or reason to consider the claimed solution and implement it as the next step in the further development of the prior art. On the contrary, “Bertozzi“ teaches away from the technical teaching of the patent-in-suit. As explained above, „Bertozzi“ expressly states that switch operation is latency insensitive in that correct operation is guaranteed for arbitrary link pipeline depth; a flexible number of stages can be inserted to decouple link throughput from its length and to get arbitrary topologies. The number of repeater stages and the length of links only depend on the pre-defined timing requirements, not the periodicity between network stations. Against this background, the skilled person,

starting from “Bertozzi“, has no reason to look for a solution for how to maintain the correct periodicity in a network when the clock speed is increased. Rather, „Bertozzi“ requires the system to be composed of modules whose behavior does not depend on the latency of input communication channels (p. 24, right col., 3rd para. of „Bertozzi“).

186 Nothing else can be inferred from the passage cited by the Defendants in the oral hearing, that “techniques have to be devised to decouple link throughput from its length and to allow functionally correct operation of the switches in presence of mis-aligned inputs due to the unequal length of the input links” (p. 23, left col., 2nd para. of “Bertozzi”). This statement is too general for directing the skilled person to implement the next step in the direction of the claimed invention. On the contrary, “Bertozzi” generally proposes a solution to overcome the interconnect-delay problem by pipelining interconnects (p. 24, right col., 3rd para. of “Bertozzi”). There does not seem to be any need to adjust the number of pipeline stages to the number of flits, especially when one considers that Bertozzi also points out that network switches can be “designed in such a way that their functional correctness depends on the flit arriving order and not on their timing” (p. 24, right col., last para. of “Bertozzi”).

(2)

187 Even if the skilled person consulted „Nowatzyk“, s/he would not arrive at the technical teaching of the patent-in-suit.

188 „Nowatzyk“ relates to point-to-point interconnect communications technologies for use in an arbitrarily assembled computer network. It discloses a preferred embodiment comprising an arbitrarily configured collection of nodes. There are point-to-point interconnections between nodes, connected to one of the serial ports of the nodes at each terminal end. During system initialisation the logic associated with each node explores each port to determine the presence of adjacent nodes. Also, during this process the signal round-trip transmission delay time between nodes is calculated for use by the communications protocol (col. 6 l. 40-52 of „Nowatzyk“).

189 With regard to the format of the data packets and their transmission, „Nowatzyk“ states that adjacent nodes continuously exchange data packets over links between corresponding coupled ports. Each data packet is of a fixed length and takes a finite amount of time to propagate toward an adjacent node. The interconnect controller incorporated in each node intelligently adjusts the transmission delay between the adjacent nodes to be equal to an integral number of packet transmission times. The mechanism for adjusting the transmission delay between adjacent nodes is called a temporal alignment buffer. Because the transmission delay between adjacent nodes over a given link is equal to an integral multiple of the time for launching a single data packet, each node knows when to expect the header of each of the continuously fed packets supplied to it (col. 6, l. 53-67 of „Nowatzyk“).

190 This shows that the nodes only work correctly if they receive the data packets in a pre-defined time. Yet, „Nowatzyk“ fails to disclose features 4.1 and 4.2 of patent claim 1 and feature 3.2 of patent claim 8. The temporal alignment buffer, which the Defendants identify as data

storage elements, is not located in a first communication channel but in the interconnect controller within the node, i.e. the network station within the meaning of the patent-in-suit. Moreover, „Nowatzyk“ does not provide any information about any correlation of the number of data storage elements within the temporal alignment buffer with the number of data elements within a data package. The function of the temporal alignment buffer is not to delay whole data packages for M*N clock cycles corresponding to the number of data elements in order to improve the clock speed and simultaneously maintain the correct periodicity. Rather, the delay depends on the “packet transmission time” which is caused by the level of network congestion or the wire length and is variable. In this respect, “Nowatzyk” follows a different concept to Bertozzi, who partitions the connections using pipeline stages. For this reason alone, skilled person would not combine the two documents, nor would they lead to the invention of the patent-in-suit.

c) BP-CR 1 (“Bertozzi”) in combination with BP-CR 3 (“Hassoun”)

191 For the reasons stated above with regard to a combination of “Bertozzi” and “Nowatzyk”, a combination of “Bertozzi” with S. Hassoun et al., “Optimal Buffered Routing Path Constructions for Single and Multiple Clock Domain Systems”, ICCAD 2002 (hereinafter: “Hassoun”) does not render the technical teaching of the patent-in-suit obvious.

192 “Bertozzi” cannot be regarded as a suitable starting point, nor is there any pointer or motivation for the skilled person that directs it to implement the next step in the direction of the claimed invention. Reference can be made to the above reasons regarding the combination of “Bertozzi” and “Nowatzyk.”

193 Irrespective of this, the skilled person would not arrive at the claimed technical teaching if it combined “Bertozzi” and “Hassoun” as the latter does not disclose feature group 4 of patent claim 1 and feature 3.2 of patent claim 8.

194 “Hassoun” addresses new problems in routing and buffer insertion, rising from shrinking process geometries and the increasing use of IP components in SoC designs. In particular, it explores routing and buffer insertion in the context of single and multiple clock domains and presents optimal and efficient polynomial algorithms that can be used to estimate communication overhead for interconnect and resource planning in single and multi-clock domain systems (see Abstract of “Hassoun”). With regard to single clock domain routing, „Hassoun“ states that

> “routing over large distances in increasingly aggressive technologies will require several clock cycles to cross the die. Hence, one must periodically clock the signal by inserting synchronization elements (such as registers) along the signal path. In this case, one cannot simply treat a register like a buffer and add the register delay to the existing path delay in the Fast Path algorithm. The realizable delay between

consecutive registers on a path will always be determined by the clock period, regardless of the actual signal propagation time." (p. 3, left col., 1st para. of "Hassoun")

195 Neither this passage, on which the Defendants essentially rely, nor the whole article discloses any relationship between the number of synchronization elements such as registers along the signal path and the number of data elements in a data package. On the contrary, the number of inserted registers depends on the desired clock cycle, and for a given length of a path, a number of clock cycles is needed to cross the path. "Hassoun" only aims to "find a feasible buffer-register path (…) such that the latency (…) is minimized" (p. 3, left col., 1st para. of "Hassoun"). This has nothing to do with delaying entire data packets in order to maintain network periodicity.

d) BP-CR 4 ("Dielissen") in combination with BP-CR 2 or BP-CR 3

196 Finally, the technical teaching of patent claims 1 and 8 is not obvious to the skilled person over a combination of Dielissen et al., "Concepts and implementation of the Philips Network-on-chip", IP-Based SoC Design 2003; S. 1-6, published on November 13, 2003 (hereinafter: "Dielissen") with "Nowatzyk" or "Hassoun".

197 It is undisputed that Dielissen does not disclose features 4.1 and 4.2 of patent claim 1 and feature 3.2 of patent claim 8, respectively. Since these features are also not disclosed by 'Nowatzyk' and 'Hassoun', the skilled person will not arrive at the claimed technical teaching anyway.

C Infringement action

198 The Infringement action is not successful on the merits.

I. Attacked embodiment

199 All Qualcomm NoC ICs having NoC interconnects that the Claimant alleges to be Arteris NoC, i.e. that contain a NoC designed using tools of the company Arteris Inc. and/or derivatives thereof, are the attacked embodiment (hereinafter: the attacked embodiment).

1. Legal principles

200 It is the Claimant who determines in the Statement of Claim which situation and circumstances the Court is to decide on in terms of location, time and substance. The underlying facts form the basis for the Court's decision and at the same time limit the court's competence to decide. In the event of a patent infringement action, the facts which are particularly relevant are those that allegedly constitute patent infringement within the meaning of Art. 25 ff. UPCA and fulfil the requirements for Court measures pursuant to Art. 56 ff. UPCA. Of particular importance in

this context, beside the infringing act, is the design of a product or process as alleged by the Claimant, which, according to the Claimant's submission, is said to comprise all the features of the asserted patent claim. This essentially represents the “attacked embodiment.” Accordingly, the “attacked embodiment” is regularly determined by the factual design of a certain product or a process with regard to the features of the invoked patent claim as asserted in the Statement of Claim. This can be a specific product specified, for example, by its product name, product sheet and technical design. However, the attacked embodiment may also comprise all products that generally have the technical features specified by the Claimant, which allegedly realise the technical teaching of the patent claim. This may also include products unknown to the Claimant or, in the case of an injunction, future products insofar as they essentially correspond to the features of the product presented by the Claimant in his Statement of Claim, which he considers decisive for the patent infringement. In such a case, it is usually sufficient if the Claimant has exemplified the infringement on a sample of the attacked embodiment. What is ultimately meant by the attacked embodiment depends on the interpretation of the Claimant’s submission. Once this has been defined it is for the Court to decide whether this attacked embodiment realises the teaching of the patent claim.

2. Case at hand

201 In the present case, the attacked embodiment is not only limited to the specific processor Snapdragon 8+ Gen. 1 but comprises all Qualcomm NoC ICs having NoC interconnects that the Claimant alleges to be Arteris NoC, i.e. include a NoC designed using tools of the company Arteris Inc. and/or derivatives thereof. The Claimant clearly states in its Statement of Claim that it is attacking products

> “that include ICs that incorporate, implement, utilize, include, or otherwise comprise NoCs designed using tools from the company Arteris Inc. (‘Arteris NoC’) or NoCs which are materially similar (core-identical) to such Arteris NoCs. These products are patent infringing ‘infringing embodiments’.” (p. 39 of the Statement of Claim)

On the preceding pages of the Statement of Claim, the Claimant has explained what it means by “NoCs designed using tools from the company Arteris Inc.” According to this, all attacked embodiments (in the Claimant’s own words: “infringing embodiments”) comprise integrated circuits (ICs) of the Defendants, having network on chip (NoC) interconnects (these are the “Qualcomm NoC ICs”). These ICs include SoCs, such as the Snapdragon 8+ Gen. 1. The Qualcomm NoC ICs comprise a network as on-chip interconnect. More particularly, the network concerns a network on chip (NoC). These NoCs include (but are not limited to) a NoC designed using tools of the company Arteris and/or derivatives thereof (these are the “Arteris NoC”). For the meaning of “Arteris NoC”, the Claimant refers to Arteris NoC Chapter submitted as Exhibit P 11. Consequently, the attacked embodiment covers all products that feature NoC which, according to the Claimant’s submission, are designed in accordance with the Arteris NoC Chapter. In this context, the mention of the Snapdragon 8+ Gen. 1 has only been made by way of example.

202 This is also clear from the fact, that, with regard to the list of specific processors and other products provided in the Statement of Claim (see p. 43 ff. of the Statement of Claim), the Claimant refers to “non-limiting examples of infringing embodiments” (p. 43 of the Statement of Claim). This shows that the attacked embodiment is not limited to the Snapdragon 8+ Gen. 1 or products expressly listed in the Statement of Claim but comprises all products in the meaning of the general definition put forward by the Claimant. The Snapdragon 8+ Gen. 1 is only the model that exemplifies the attacked embodiment and on the basis of which the Claimant attempts to demonstrate infringement of the patent-in-suit.

203 It follows from this, that the attacked embodiment in any case covers all of the Defendants’ products listed in the Statement of Claim, but is not limited to them. The single exception is the processor MSM6000, which the Defendants contest as falling within the Claimant’s definition of the attacked embodiment as it uses a different technology than the processor Snapdragon 8+ Gen. 1 and does not even have a NoC. The Defendants have not disputed that other processors fall within the scope of the definition of the attacked embodiment. In this respect, the Claimant's simple assertion that all the other listed models are corresponding processors is sufficient. It would have been incumbent on the Defendants to dispute this for certain models on the list. This is reasonable for them because they know their own products best. Instead, however, they have merely made unsubstantiated claims that there were other models on the list which were already publicly available before the priority date of the patent-in-suit without using any NoC technology. This is not sufficient to dispute the Claimants’ assertion.

204 The Samsung Galaxy smartphones, chromebooks, laptops and tablets, which the Claimant refers to as “infringing embodiments IV” by the Claimant, do not constitute a further attacked embodiment. Since they contain processors that constitute the attacked embodiment they do not differ from the attacked embodiment in technical terms or in terms of the features relevant to the realisation of claim 1 of the patent-in-suit. Rather, the arrangement of these processors in electronic devices and the offering and distributing of these devices by companies other than the Defendants raises questions with regard to the infringing acts and the perpetration and participation in such acts.

II. Realisation of claim features

205 The attacked embodiment is not the subject matter of claim 1 within the meaning of Art. 25 (a) UPCA, nor is it obtained directly by a process which is the subject matter of claim 8 within the meaning of Art. 25 (c) UPCA.

206 The Claimant asserts that the attacked embodiment comprises NoC designed using tools developed by Arteris and described in the Arteris NoC Chapter (Exhibit P 11), in particular using the Danube IP library. The Defendants have contested the use of Arteris NoC and tools described in the Arteris NoC Chapter. However, the Claimant's submission based on the

Arteris NOC Chapter is already inconclusive. In addition, the realisation of the technical teaching of the patent-in-suit cannot be established on the basis of the Defendants' submission regarding the functioning of the attacked embodiment.

1. Assessment based on Arteris NoC chapter

207 It cannot be established that the attacked embodiment comprises NoC designed using tools developed by Arteris and described in the Arteris NoC Chapter (Exhibit P 11), in particular using the Danube IP library. The Claimant's submissions submissions based on the Arteris NOC Chapter are already inconclusive.

a) Data package comprising N data elements

208 A NoC designed using tools developed by Arteris and described in the Arteris NoC does not realise feature 2.1.1 of claim 1 of the patent-in-suit.

209 The Claimant considers data packets according to the Arteris NoC chapter as data packages within the meaning of feature 2.1 of claim 1. This cannot be objected and is not disputed by the Defendants, because these data packets represent a meaningful data unit including routing information. The Arteris NoC Chapter reads:

> "All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (…). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address." (p. 313 of Exhibit P 10).

The structure of the data packet is shown below in Figure 11.2 of the Arteris NoC Chapter:

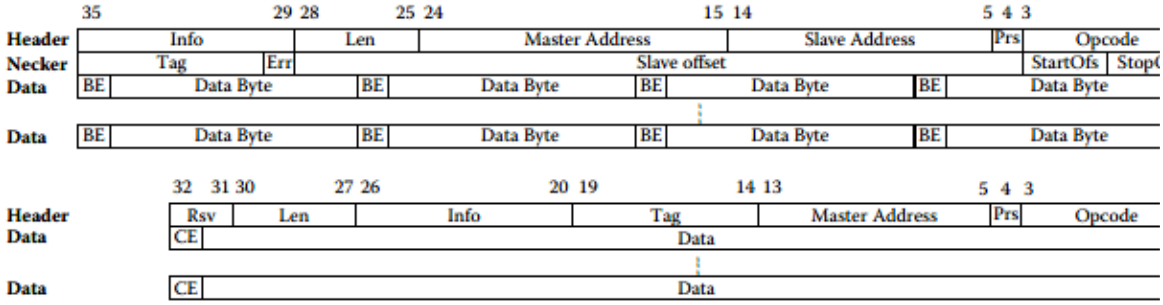

FIGURE 11.2
NTTP packet structure.

210 The Claimant considers the cells to be data elements within the meaning of claim 1. However, it can already be seen from the quoted passage that the data packets have a variable size as the necker cell is optional and the number of data cells as well. It already follows from this that not every data packet comprises a fixed number of N data elements in accordance with feature 2.1.1.

211 This is also confirmed if the data units transferred per clock cycle are taken into account that might constitute data elements within the meaning of feature 2.1.1 of claim 1. The Arteris NoC Chapter states in this regard:

> “The delivery of packets within the NoC is the responsibility of the physical layer. Packets, which have been split by the transport layer into cells, are delivered as words that are sent along links. Within a single clock cycle, the physical layer may carry words comprising a fraction of a cell, a single cell, or multiple cells. The link size, or width (i.e., number of wires), is set by the designer at design time and determines the number of cells of one word. NTTP defines five possible link-widths: quarter (QRT), half (HLF), single (SGL), double (DBL), and quad (QUAD). A single-width (SGL) link transmits one cell per clock cycle, a double-width link transmits two cells per clock cycle, and so on.” (p. 313 of Exhibit P 10)

212 According to this, the data unit transmitted per clock cycle depends on the link-widths and consists of one word that may correspond to a fraction of a cell (1/4 or 1/2), one cell or more than one cells (2 or 4). In any event, since the number of cells in a data packet varies, the number of data elements in a data packet also varies, regardless of whether the data element is a fraction of a cell, one cell or more than one cell. Feature 2.1.1 is in each case not realized. The Claimant's differing opinion is based solely on its claim interpretation, which cannot be accepted here.

213 Insofar as the Claimant referred to Figure 11.1 of the Arteris NoC Chapter for the first time in the oral hearing and argued that the links between the NIUs for transmitting the request and response packets each established subnetworks within which the number of transmitted cells was always the same, this is not convincing. As can be seen from the preferred embodiments of the patent-in-suit, the individual network stations require that the periodicity of the network be maintained. Connections for incoming and outgoing packets between two stations are referred to as subchannels in the patent-in-suit and together these subchannels constitute the communication channel within the meaning of the patent at issue and feature 4 (see para. [0027], [0028], [0031]). The individual subchannels of a communication channel may have fewer than M*N data storage elements, but the sum of the data storage elements in the entire communication channel must be M*N according to feature 4. However, this also means that the periodicity for incoming and outgoing packets of a network station is identical and subchannels cannot be regarded as subnetworks. Therefore, all data packages, regardless of which subchannel they are transmitted on, must have exactly N data elements. But even the Claimant asserts this.

214 Notwithstanding, it cannot even be inferred from the Arteris NoC Chapter that all request packets have the same number of cells and data elements, respectively. The same is applies to response packets. Regardless of the type of the packet, the Arteris NoC Chapter states: “All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells” (p. 313 of Exhibit P 10). The Arteris NoC Chapter does not even require

periodicity of the network. Insofar as the Claimant refers to figure 11.3 of the Arteris NoC Chapter and the number of “n” data cells, nothing else applies, since “n” must be understood as a variable that can vary within the network.

b) Communication channel comprising M*N data storage elements

215 Furthermore, the Claimant has not demonstrated that the attacked embodiment realizes feature group 4.

216 In order to demonstrate that feature group 4 is implemented by the attacked embodiment, the Claimant refers to several electronic components that are allegedly present or could be present in the attacked embodiment. However, the Claimant never explains how many of these supposed data storage elements are to be arranged in a communication channel of the attacked embodiment. Features 2.1.3 and 4.1 indicate that there must be at least two. The Claimant does not comment on this. This is also not possible because, according to the Arteris NoC Chapter, the data packets have a variable number of data elements. Accordingly, there is also no fixed number of M*N of data storage elements in one communication channel of the attacked embodiment.

(1)

217 First the Claimant relies on delay pipelines to show that feature group 4 is realized. The corresponding passage in the Arteris NoC Chapter reads:

> “Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput.” (p. 322 of Exhibit P 10)

218 However, as is already apparent from the quoted text itself, delay pipelines are not used to delay whole data packages within the meaning of feature 4.2. Rather, their function is to keep the data information in phase with the routing information. Since the latter is processed by the input controller, which may require more than one cycle, a delay pipeline is necessary to delay data information and thus restore the phase between data information and routing information. However, this does not mean that the whole data package is delayed by at least N clock cycles or a multiple thereof.

219 It follows that, as the Defendants rightly point out with reference to Figure 11.6 of Exhibit 10, the delay pipelines are inserted in the input controller and are part of the router or switch itself, not the first communication channel as required by feature group 4. The patent-in-suit differentiates between storage elements arranged inside a switch or router (see para. [0019]) and inside the communication channel. Claim 1 is limited to M*N data storage elements arranged in a first communication channel.

(2)

220 The Claimant further refers to different packet transportation units representing different hardware modules used to route, transmit over a long distance, and adapt data flows with different characteristics, like “muxes”, “synchronous FIFOs” and “width and endian converters”, which are mentioned in the Arteris NoC Chapter (p. 319 of Exhibit 10).

221 However, the Claimant does not specify which specific unit is implemented in the attacked embodiment. The packet transportation units are provided by the Arteris Danube library and may be inserted in a NoC, but they are not necessarily part of the attacked embodiment. Furthermore, the Claimant does not state how many of these units are inserted in one communication channel of the attacked embodiment. Thus, it is not stated, nor is it apparent that a first communication channel of the attacked embodiment comprises M*N data storage elements for delaying whole data packages.

(3)

222 The Claimant also refers to input pipes introducing FIFOs, which help timing closure. The corresponding paragraph in the Arteris NoC Chapter reads as follows:

> „The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle.“ (see p. 322 of Exhibit P 10)

This section also refers to the routers and switches, whereby the input pipes are not inserted into a first communication channel but rather into these routers and switches, like the delay pipelines. In addition, the input pipe contains a one-word-deep FIFO, hence providing a delay of one clock cycle, as is known from the prior art, but not of an entire data package as required by feature group 4.

(4)

223 Insofar as the Claimant refers to a parameter called “fwdPipe” mentioned in section 11.3.4.1 of the Arteris NoC Chapter, realisation of claim feature 4 is not demonstrated. The corresponding section reads:

> “The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path.” (p. 323 of Exhibit 10)

224 As can be seen from the text, D flip flops (DFFs) are inserted which register a data word as well as control signals. Thus, it is only stated that one word is delayed, not a whole data package, which is also indicated by the passage “a cycle delay is inserted.” According to

section 11.3.1.3 of the Arteris NoC Chapter, the (data) word comprising a fraction of a cell, a single cell, or multiple cells, is delivered within a single clock cycle and corresponds to the data element within the meaning of the patent claims. This (data) word has to be distinguished from the data packet, which, according to section 11.3.1.2 of the Arteris NoC Chapter, is comprised of several cells and corresponds to a data package within the meaning of the patent claims.

225 The first time in the oral hearing, the Claimant asserted that the data word mentioned in the above-cited passage of section 11.3.4.1 of the Arteris NoC Chapter corresponds to the data package within the meaning of the patent-in-suit, since it also comprises control signals. However, Claimant's understanding of section 11.3.4.1 and the terms "data word", "control signals", and "cycle delay for packets" contradicts the definition of data packets, words and cells in sections 11.3.1.2 and 11.3.1.3 of the Arteris NoC Chapter. The term "data word" is used again in section 11.3.3.1 of the Arteris NoC Chapter in connection with switching and is apparently synonymous with the term "word" defined in section 11.3.1.3 of the Arteris NoC Chapter, as it is transferred within a single clock cycle. The "control signals" mentioned in section 11.3.4.1 of the Arteris NoC Chapter appear to be the signals defined for the physical layer in section 11.3.1.3 of the Arteris NoC Chapter, as are the (data) words. However, these signals are not routing information within the meaning of feature 2.1.2.

226 As a result, a data word including control signals cannot be regarded as a data package according to feature group 2.1 of the patent claims, and the above-cited passage in section 11.3.4.1 of the Arteris NoC Chapter merely describes the insertion of DFFs which delay one data word (including control signals) on the physical layer by one (or more) clock cycles. Consequently, the data packet delivered as words is also delayed by one (or more) clock cycles. However, the Arteris Noc Chapter and the above-cited passage do not require that M*N DFFs, which correspond to the data storage elements, be inserted, nor that the data packet be delayed by M*N clock cycles.

227 Furthermore, the Defendants point out that the insertion of the fwdPipe parameter is optional and in the user's responsibility. It is not mandatory to insert a number of pipeline registers corresponding to a delay of M*N cycles, i.e. a whole data package. The Claimant does not demonstrate that such a delay occurs as a result of the insertion of the fwdPipe parameter in the attacked embodiment. The mere reference to the Arteris NoC Chapter and the possibility of inserting DFFs using the fwdPipe parameter is not sufficient and therefore inconclusive

(5)

228 The same applies insofar as Claimant refers to other presentations of Arteris about their NoC technology submitted as Exhibits P 12 and P 13, which describe adding a number of pipeline stages according to the length of the wire, i.e. physical distance between start and end. Even if the pipeline stages are data storage elements within the meaning of claim 1, nothing is stated, nor is it apparent, that the number of these data storage elements to be inserted into the communication channel corresponds in any way to the number of data elements in a data package. This does not appear to be necessary either, since according to the Arteris NoC

Chapter, the data packages have a variable size, i.e. a variable number of data elements, and a delay of one clock cycle may be sufficient, as was known from the prior art.

(6)

229 The Claimant's afore-mentioned references to the Arteris NoC chapter were only elaborated on in the Reply to the Statement of Defence with regard to the width converter and the rate adapters. However, width converters and rate adapters cannot be considered data storage elements for delaying whole data packages including the routing information by introducing a delay of M*N cycles on the first channel.

230 A width converter converts signals from a larger signal path to a smaller signal path and vice versa. For example, a 32-bit word sent in one clock cycle on a 32-bit signal path is split into four 8-bit words that are sent in four clock cycles. Conversely, four 8-bit words sent in four clock cycles can be combined into a 32-bit word and sent in one clock cycle. Even if the latter width converter may contain data storage elements, it is immediately apparent that width converters do not delay whole data packages by M*N clock cycles. Rather, every data element is delayed by another number of clock cycles. In the case of a conversion from 8-bit signals to 32-bit signals, the first 8-bit word must be delayed until the last 8-bit word arrives in order to send them together as a 32-bit signal. Even if the 32-bit word is considered one data package, this package is not delayed by four clock cycles as it can immediately be send after arrival of the last 8-bit word. Feature group 4 is not realised.

231 The same applies to rate adapters which, according to the Claimant, function similarly to width converters albeit adapting the rate at which data is transported instead of the data width.

(7)

232 For the reasons stated above, the Claimant’s reference to drivers of the Linux kernel does not constitute a conclusive explanation for the realisation of feature 8 of claim 1 as the Claimant merely concludes the existence of width and rate converters from parts of the Linux Kernel source code. Width converters and rate converters cannot be regarded as M*N data storage elements for delaying whole data packages by introducing a delay of M*N cycles within the meaning of claim 1.

c) Consequences for claim 8

233 The features of claim 8 of the patent-in-suit correspond to those of claim 1 so that it cannot be established for the reasons stated above that the attacked embodiment was designed using the method of claim 8.

234 Furthermore, the Claimant has not stated, nor is it apparent that, when designing the attacked embodiment, a first communication channel was identified within the meaning of feature 3.1 of claim 8.

2. Assessment based on Defendants' submissions

235 An infringement of the patent-in-suit can also be ruled out if one follows the Defendants' argument that the attacked embodiment does not use the technology according to Arteris.NoC Chapter.

236 The Defendants have stated and confirmed in a written witness statement of [redacted] former Arteris employee and with Qualcomm since 2013, currently employed as a Senior Director and inter alia responsible for designing parts of the technology used in Qualcomm's proprietary NoCs, how data packets are transmitted and delayed in the attacked embodiment. According to this, NoCs in Qualcomm products transmit data packets. Each data packet consists of one or more words. A word is a fixed-size group of bits equal to the size of the data bus the word is being transmitted on. [redacted], i.e. the data packets do not all contain the same number of words. [redacted], the routing information does not arrive at the network interfaces or routers/switches at any defined, consistent interval.

a) Data package comprising N data elements

237 It is not necessary to decide whether the attacked embodiment, as presented by the Defendants, differs from the technology described in the Arteris NoC chapter with regard to the disputed claim features. In any case, the contested embodiment does not realise feature 2.1.1 of claim 1 because, even according to the Defendants' submission, [redacted]. The data packets consist of one or more words. These correspond to the data elements within the meaning of feature 2.1.1 because a word is a fixed-size group of bits equal to the size of the data bus the word is being transmitted on, thus transmitted during one clock cycle. Since the data packets do not all contain the same number of words, feature 2.1.1 is not implemented.

b) Communication channel comprising M*N data storage elements

238 The Defendants have also disputed realisation of feature group 4 of claim 1 by the attacked embodiment. They state that [redacted].

239 This corresponds to the findings regarding the Arteris NoC Chapter and the Defendants' statements regarding features 2.1.1 to 2.1.3 according to which the data packages have various numbers of data elements. Against this background, a fixed number of M*N data

storage elements does not make sense for the delay of whole data packets. In other words, it has not been demonstrated, nor is it apparent, that there is a fixed number of M*N of data storage elements that is a multiple of a fixed number N of data elements of all data packages and vice versa. Even if it cannot be ruled out in individual cases that the number of data storage elements in a communication channel of the attacked embodiment happens to be a multiple of the number of data elements of individual data packages, this is not sufficient for the realisation of the technical teaching of the patent-in-suit.

240 Furthermore, the Defendants have conceded that width converters and rate converters are implemented in the attacked embodiment. However, as already mentioned, such components cannot be regarded as data storage elements for delaying whole data packages by introducing a delay of M*N cycles on the first communication channel. The Defendants have additionally explained why these converters cannot realise feature group 4 due to their design.

(1)

241 [redacted]. Even the Claimant does not dispute that a multiplexer is not a data storage element for delaying whole data packages by M*N clock cycles. However, the functioning of the second type of width converters also excludes the realisation of feature group 4.

242 The Defendants explain that [redacted], for example [redacted]. Even if, in the example, the four 8-bit chunks on the first 8-bit signal path are regarded as a data package comprising four data elements (N = 4), the width converter of the attacked embodiment comprises [redacted] not M*4 data storage elements in accordance with feature group 4. According to the general formula, it is excluded that the number of registers corresponds to the number of data elements in a data package or a multiple thereof.

(2)

243 The Defendants have also conceded that some types of the attacked embodiment use rate adapters that connect a signal path having a lower rate to a signal path having a higher rate. [redacted].

244 Based on this statement of the Defendants, the realisation of feature group 4 is excluded. As already explained, a rate adapter does not delay the entire data package by M*N clock cycles

but buffers the individual data elements for different lengths of time (those arriving first for longer than those arriving later) and then sends them one after the other on the second path at a higher transmission rate. However, this does not delay the whole data packet uniformly, and certainly not by M*N clock cycles. Since the data packets have a different number of data elements and thus a different size, there is also no fixed assignment between the varying number N of data elements in the data package and the fixed number of data storage elements in the form of M*N data storage elements in accordance with feature group 4. In this respect, the same applies to rate adapters as to width converters.

c) Consequences for claim 8

245 The features of claim 8 of the patent-in-suit correspond to those of claim 1 so that it cannot be established for the reasons stated above that the attacked embodiment was been designed using the method of claim 8.

3. Equivalence

246 The use of the technical teaching of claim 1 according to the principles of equivalence must be denied.

247 It is not necessary to decide what the specific requirements of the principles of equivalence are (see LD The Hague, Decision of 22 November 2024, UPC_CFI_239/2023 – Plant-e/Arkyne; LD Brussels, Decision of 17 January 2025, UPC_CFI_376/2023 – OrthoApnea; LD Mannheim, Decision of 6 June 2025, UPC_CFI_471/2023 – DISH/Aylo), since the Claimant has not specifically explained, with regard to the attacked embodiment, which feature of the patent claim is allegedly realised by which substitute means. It only argues:

> "As shown above, feature 1.8 is literally infringed. However, in the unlikely event that the court would rule otherwise, e.g., because the court would rule that the M times N data storage elements introducing the delay of M times N cycles are not in the communication channel, but at least partly in the routers or other components of the Arteris NoC, the [Qualcomm] NoC ICs infringe feature [group 4] by equivalence."

248 However, the court does not justify non-infringement by the fact that the data storage elements are not in the communication channel. Rather, the patent-in-suit is not infringed as the data packages comprise a various number of data elements (feature 2.1.1) and no correlation between the number of data storage elements and the number of data elements is either stated or otherwise apparent (feature group 4). In this regard, however, the Claimant has not stated any alternative means, its functioning and its technical effect for the attacked embodiment.

249 Insofar as the Claimant refers to paragraph [0009] of the patent specification, this is also unsuccessful. This paragraph proposes a specific solution for a phase shift during the routing

evaluation phase. It has not been demonstrated that this is implemented in the attacked embodiment. Nor can the Claimant successfully argue that the periodicity between the network stations is maintained in the attacked embodiment. Periodicity in the attacked embodiment cannot be assumed because data packets of different sizes are used.

250 The Claimant was therefore right not to return to the infringement by means of equivalence in its Reply to the Statement of Defence.

4. Application to produce evidence

251 It follows from the reasons stated above that the Claimant's application to produce evidence is not successful and must be rejected.

a) Parties' submissions

252 The Claimant is of the opinion that it has described and substantiated the patent infringement in detail. The outline of infringement is based on the fact that the design of the Defendants' NoC ICs equals the Arteris NOC technology described in Arteris NoC Chapter. It is undisputed that the Defendants have used Arteris technology in their infringing embodiments for over a decade and the Defendant 4) hired approximately 43 Arteris engineers and acquired certain Arteris SoC technology and IP in 2013. However, Defendants stated that the Arteris NoC chapter does not fully describe the NoCs on the Defendants' infringing embodiments and claim that the details of the Arteris NoC technology differs from the design used for the Qualcomm NoCs. The Claimant argues that the Defendants should be ordered to produce evidence, in particular the source code and the technical documents of the infringing embodiments, since Claimant has presented the Arteris NoC Chapter as evidence in support of its claims and does not have access to any other available evidence whereas the Defendants know and have access to these documents, as these have already been produced by the Defendants in the parallel US proceedings pending with the Western District of Texas.

253 The Defendants argue that the Claimant has not sufficiently specified any evidence to be produced. The sheer volume of data related to the source code already shows that Claimant's request is not aimed at obtaining specific evidence for showing the use of a certain claim feature, but a comprehensive US style discovery, a so-called "fishing expedition", which Rule 190 RoP does not support. Furthermore, Claimant has not specified which facts should be evidenced by the requested information. Finally, the Claimant has failed to show that the evidence to be produced by Defendants serves to substantiate the alleged infringement claim. In the Defendants' view, the Claimant has not even presented its infringement claim conclusively.

b) Requests

254 Originally, the Claimant requested, that the Defendants 3), 4) and 5) are ordered to produce the source code and the internal and external technical documents of (I.) the System on Chip (SoC) architecture of the infringing embodiments, (II.) the infringing embodiments, evidencing the communication between the processing modules through the NoC interconnect, and (III.) the infringing embodiments, evidencing how Quality of Service (QoS) is supported and managed in Defendants NoC infrastructure.

255 Later, the Claimant amended its application and now requests:

I. The so-called "Qualcomm source code" which is specifically identified and individually addressed in the Western District of Texas Action Order dd. 26 November 2024 – see Network System Technologies, LLC v. Qualcomm Inc. et al., Case No. 1:22-cv-1331-DAE, Dkt. 259, – whereas the evidence production may be performed by (1) producing to Claimant the paper printouts of the source code already generated and provided to Claimant in the Western District of Texas WDTex Action, and by (2) allowing Claimant's party expert [redacted] access to the aforesaid "Qualcomm source code" and access to these paper printouts, and by disclosing the "Qualcomm source code" to him again at the premises of ProSearch's Secure Facility, located at 3250 Wilshire Blvd., Los Angeles, CA 90010, USA, where it is currently stored and displayed for the purpose of production of evidence in the Western District of Texas Action, and by allowing Claimant's party expert [redacted] to document and to describe the "Qualcomm source code", for example, by taking and making written notes and requesting printouts;

II. The so-called "NST supplemental infringement contentions" which are specifically identified and individually addressed in the Western District of Texas Action Order dd. 26 November 2024 and that were amended by Claimant on 7 February 2025, as stated in Claimant's Notice of Compliance – see Network System Technologies, LLC v. Qualcomm Inc. et al, Case No. 1:22-cv-1331-DAE, Dkt. 292; and

III. The "documents" which are specifically identified and individually addressed by Claimant in Claimant's 7 February 2025 "NST supplemental infringement contentions" – see Network System Technologies, LLC v. Qualcomm Inc. et al, Case No. 1:22-cv-1331-DAE, Dkt. 292.

256 The Defendants request that

Claimant's "Amendment of Request pursuant to R. 190 RoP" be dismissed.

c) Grounds

257 The Claimant's request for an order to produce evidence has no basis in Art. 59 (1) UPCA and Rule 190.1 RoP and is therefore unfounded.

(1)

258 According to Art. 59 (1) UPCA and Rule 190.1 RoP, the Court may, where a party has presented reasonably available and plausible evidence in support of its claims and has, in substantiating those claims, specified evidence which lies in the control of the other party or a third party, on a reasoned request by the party specifying such evidence, order that other party or third party to produce such evidence. For the protection of confidential information, the Court may order that the evidence be disclosed to certain named persons only and be subject to appropriate terms of non-disclosure

259 In accordance with the case law of the Court of Appeal ("CoA") of the UPC, as also adopted by different Local Divisions, the following principles apply to a request under Rule 190 RoP.

260 As a rule, an order to produce evidence presupposes that there is a fact that is relevant to the substantiation of claims (or defences) and that the fact requires proof by the party who is making the application (also cf. the CoA referred to above, para. 36, explaining that the purpose of these provisions is to ensure that the party who has the burden of proof will have access to the tools for carrying this burden). To this end, the applicant must set out in the application which fact it wishes to prove by which means of evidence and for what reason. No evidence is required for a fact that is not (specifically) contested (see Rule 171.2 RoP). If a fact is not relevant to the claims (or defences) being pursued, ordering the production of evidence for such a fact is generally at least disproportionate (CoA, Order of 24 September 2024, UPC_CoA_298/2024 – Panasonic/Oppo; LD Mannheim, Order of 20 October 2024, UPC_CFI_471/2023 – Dish/Aylo; LD Munich, Order of 3 April 2025, UPC_CFI_846/2024 – Promosome/BionTech).

261 An applicant for an order pursuant to Rule 190 RoP must have presented reasonably available and plausible evidence in support of its claims (or defences) before an application under Rule 190 RoP can be granted. Whether the applicant has met this requirement and, as a result, whether an order to evidence against the opponent or a third party can be considered is at the discretion of the Court. When exercising this discretion, the circumstances of the individual case must be taken into account, taking into account the mutual interests and the principle of efficient conduct of proceedings (CoA, Order of 24 September 2024, UPC_CoA_298/2024 – Panasonic/Oppo; LD Mannheim, Order of 20 October 2024, UPC_CFI_471/2023 – Dish/Aylo; LD Munich, Order of 3 April 2025, UPC_CFI_846/2024 – Promosome/BionTech).

262 The burden of presentation and proof for the existence of the prerequisites for an order to produce evidence, lies with the applicant (CoA, Order of 24 September 2024, UPC_CoA_298/2024 – Panasonic/Oppo; LD Mannheim, Order of 20 October 2024,

UPC_CFI_471/2023 – Dish/Aylo; LD Munich, Order of 3 April 2025, UPC_CFI_846/2024 – Promosome/BionTech).

(2)

263 Applying the above principles to the present case, the Court exercises its discretion not to issue an order to produce evidence. The Claimant's requests are not well-founded.

264 The Claimant has already failed to present any plausible evidence to support its claim. The allegation of the infringement of the patent-in-suit is based solely on the Arteris NoC Chapter and the fact that the Defendants have acquired Arteris technology and have been using it for some time. However, the Arteris NoC chapter does not constitute plausible evidence for the Claimant's assertion. As already mentioned, the Arteris NoC chapter does not constitute conclusive evidence of infringement. Even if one were to assume that only individual features cannot be proven, it must be taken into account that the Claimant based its case from the outset on the Arteris NoC chapter and the assertion that this proves the infringement of the patent-in-suit. In doing so, the Claimant could not even assume that the Arteris NoC chapter describes the functionality of the attacked embodiment because the Arteris NoC Chapter does not originate from the Defendants nor does it refer to the Defendants' ICs and chips. The Claimant concludes that the technology described in the Arteris NoC Chapter is used solely because there have been connections between Arteris and the Defendants in the past (acquisition of technology, takeover of employees and the like). From a technical point of view, this is completely unspecific for the infringement of the patent-in-suit. The Claimant could not assume that the Arteris technology Defendants acquired was identical to the details described in the Arteris NoC Chapter. Rather, it can be presumed that, as the Defendants also argue, Arteris and the Defendants each use proprietary technology that differs in key aspects.

265 Furthermore, the Defendants also disputed the use of technology according to the Arteris NoC Chapter and even explained the different mode of operation. Only then did the Claimant request the submission of the source code. At that time, and even now, the Arteris NoC Chapter appears completely implausible, also in view of the Defendants' submissions. The Claimant entered the proceedings on the basis of the Arteris NoC Chapter with a mere assumption about the functionality of the attacked embodiment, and this assumption proved to be untenable. There is more to suggest that request for the production of the source code only serves to find a new justification for the infringement claim or ultimately confirms the Defendant's submission. However, an order to produce evidence pursuant to Rule 190.1 RoP does not serve this purpose. It already lacks a plausible evidence in support of Claimant's claim.

266 The application to produce evidence is ultimately aimed at finding out how the attacked chips possibly work. Based on claims 1 and 8 of the patent in suit, the Claimant does not specify any individual features or functionalities of the chips that are still missing for the purpose of proving patent infringement and for which specific evidence is to be presented. The sheer volume of documents that are the subject of the application for production of evidence indicates that the allegation of infringement was made completely in the dark and that the

application was filed in the hope of finding any evidence of a possible infringement. This is further indicated by the fact that the application does not differ in any way from the applications in the parallel proceedings, even though different technologies are involved.

267 Against this background, the requested order cannot be granted. This is without even taking into account the fact that the source code to be inspected contains highly sensitive technical trade secrets of the Defendants, the disclosure of which should not be ordered without good reason, even taking into account possible confidentiality measures.

268 The Claimant's statement during the oral hearing that this is a classic case for the submission of the source code in accordance with Rule 190 RoP cannot be accepted for the reasons stated above. For these reasons, the witnesses offered by the Claimant were also not heard. The Claimant's objection that the Defendants only presented a written witness statement and that the witness was not heard at all is not valid. The Claimant bears the burden of proof for the alleged infringement and has not presented its claim in a conclusive manner. In this respect, the mere dispute by the Defendants was sufficient.

269 Insofar as the Claimant indicated in the oral hearing that the request for the production of evidence could have been decided earlier and, in any case, instructions could have been given if there was a lack of plausible evidence, this cannot be accepted. In the present case, a decision on the application under Rule 190 RoP could only be made after comprehensive preparation of the case. If a production of evidence had been considered, the hearing could have been adjourned or reopened. However, even in the oral hearing, the Claimant did not present any further facts or possible evidence to make its claim conclusive or even to substantiate it.

DECISION

1. The Infringement action is dismissed.

2. The Counterclaim for revocation is dismissed.

3. The costs of the Infringement action against the Defendants 3) to 5) are to be borne by the Claimant. The costs of the Counterclaim for revocation are to be borne by the Defendants 3) to 5).

4. The value in dispute for the Infringement action is set at EUR 8,000,000. The value in dispute for the Counterclaim for revocation is set at EUR 12,000,000.

On behalf of the Presiding Judge Ulrike Voß, in her absence: Daniel Voß (Legally Qualified Judge)	
Daniel Voß (Legally Qualified Judge)	
Pierluigi Perrotti (Legally Qualified Judge)	
Andrea Scilletta (Technically Qualified Judge)	
For the sub-registrar	

INFORMATION ON APPEAL

An appeal against this decision may be brought before the Court of Appeal by any party whose claims have been unsuccessful, in whole or in part, within two months of service of the decision (Art. 73(1) UPCA, R. 220.1 (a) RoP, 224.1 (a) RoP).

INFORMATION ON ENFORCEMENT (ART. 82 UPCA, ART. 37(2) UPCS, R. 118.8, 158.2, 354, 355.4 ROP)

An authentic copy of the enforceable order will be issued by the Deputy-Registrar upon request of the enforcing party, R. 69 RegR.

This decision was read in open court on 11 March 2026.

Note

This document is a redacted version of the Decision, with confidential information removed. It is valid without the signatures of the judges involved and the representative of the Sub-Registrar.

Daniel Voß Digital unterschrieben von Daniel Voß Datum: 2026.03.11 11:10:01 +01'00'